19-3501; Rev 0; 11/04

EVALUATION KIT AVAILABLE

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

General Description

The MAX1533/MAX1537 are dual step-down, switch-mode power-supply (SMPS) controllers with synchronous rectification, intended for main 5V/3.3V power generation in battery-powered systems. Fixed-frequency operation with optimal interleaving minimizes input ripple current from the lowest input voltages up to the 26V maximum input. Optimal 40/60 interleaving allows the input voltage to go down to 8.3V before duty-cycle overlap occurs, compared to 180° out-of-phase regulators where the duty-cycle overlap occurs when the input drops below 10V. Output current sensing provides accurate current limit using a sense resistor. Alternatively, power dissipation can be reduced using lossless inductor current sensing.

Internal 5V and 3.3V linear regulators power the MAX1533/MAX1537 and their gate drivers, as well as external keep-alive loads, up to a total of 100mA. When the main PWM regulators are in regulation, automatic bootstrap switches bypass the internal linear regulators, providing currents up to 200mA from each linear output. An additional 5V to 23V adjustable internal 150mA linear regulator is typically used with a secondary winding to provide a 12V supply.

The MAX1533/MAX1537 include on-board power-up sequencing, a power-good (PGOOD) output, digital soft-start, and internal soft-shutdown output discharge that prevents negative voltages on shutdown. The MAX1533 is available in a 32-pin 5mm x 5mm thin QFN package, and the MAX1537 is available in a 36-pin 6mm x 6mm thin QFN package. The exposed backside pad improves thermal characteristics for demanding linear keep-alive applications.

Applications

2 to 4 Li+ Cells Battery-Powered Devices

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1533ETJ	-40°C to +85°C	32 Thin QFN 5mm x 5mm
MAX1533ETJ+	-40°C to +85°C	32 Thin QFN 5mm x 5mm
MAX1537ETX	-40°C to +85°C	36 Thin QFN 6mm x 6mm
MAX1537ETX+	-40°C to +85°C	36 Thin QFN 6mm x 6mm

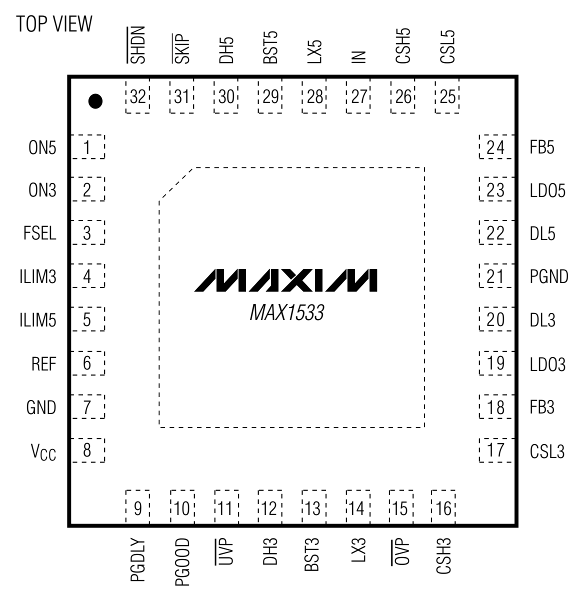
+Denotes lead-free package.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ Fixed-Frequency, Current-Mode Control
- ♦ 40/60 Optimal Interleaving
- ♦ Accurate Differential Current-Sense Inputs
- ♦ Internal 5V and 3.3V Linear Regulators with 100mA Load Capability
- ♦ Auxiliary 12V or Adjustable 150mA Linear Regulator (MAX1537 Only)
- ♦ Dual-Mode™ Feedback—3.3V/5V Fixed or Adjustable Output (Dual Mode) Voltages
- ♦ 200kHz/300kHz/500kHz Switching Frequency
- ♦ Versatile Power-Up Sequencing
- ♦ Adjustable Overvoltage and Undervoltage Protection
- ♦ 6V to 26V Input Range
- ♦ 2V ±0.75% Reference Output
- ♦ Power-Good Output
- ♦ Soft-Shutdown
- ♦ 5µA (typ) Shutdown Current

Pin Configurations



THIN QFN
5mm x 5mm

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, INA, LDOA to GND ....-0.3V to +30V
GND to PGND ....-0.3V to +0.3V
LDO5, LDO3, V_{CC} to GND ....-0.3V to +6V
ILIM3, ILIM5, PGDLY to GND...................................-0.3V to +6V
CSL3, CSH3, CSL5, CSH5 to GND ....-0.3V to +6V
$\overline{ON3}$, $\overline{ON5}$, $\overline{FB3}$, FB5 to GND ....-0.3V to +6V
$\overline{SKIP}$, $\overline{OVP}$, $\overline{UVP}$ to GND..-0.3V to +6V
PGOOD, FSEL, ADJA, ONA to GND ....-0.3V to +6V
REF to GND ....-0.3V to (V_{CC} + 0.3V)
DL3, DL5 to PGND.................................-0.3V to (V_{LDO5} + 0.3V)
BST3, BST5 to PGND ....-0.3V to +36V
LX3 to BST3..-6V to +0.3V
DH3 to LX3 ....-0.3V to (V_{BST3} + 0.3V)
LX5 to BST5..-6V to +0.3V
DH5 to LX5 ....-0.3V to (V_{BST5} + 0.3V)
LDO3, LDO5 Short Circuit to GND ....Momentary
REF Short Circuit to GND ....Momentary
INA Shunt Current...+15mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 21.3mW/°C above +70°C) 1702mW
36-Pin TQFN (derate 26.3mW/°C above +70°C) 2105mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES (Note 1)						
V_{IN} Input Voltage Range	V_{IN}	LDO5 in regulation	6		26	V
		IN = LDO5, V_{OUT5} < 4.43V	4.5		5.5	
V_{IN} Operating Supply Current	I_{IN}	LDO5 switched over to CSL5		15	35	µA
V_{IN} Standby Supply Current	$I_{IN(STBY)}$	V_{IN} = 6V to 26V, both SMPS off, includes $I_{\overline{SHDN}}$		100	170	µA
V_{IN} Shutdown Supply Current	$I_{IN(SHDN)}$	V_{IN} = 6V to 26V, $\overline{SHDN}$ = GND		5	17	µA
Quiescent Power Consumption	P_Q	Both SMPS on, FB3 = FB5 = $\overline{SKIP}$ = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V, V_{INA} = 15V, I_{LDOA} = 0, P_{IN} + P_{CSL3} + P_{CSL5} + P_{INA}		3.5	4.5	mW
V_{CC} Quiescent Supply Current	I_{CC}	Both SMPS on, FB3 = FB5 = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V		1.1	2.1	mA
MAIN SMPS CONTROLLERS						
3.3V Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)	3.280	3.33	3.380	V
5V Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)	4.975	5.05	5.125	V
Feedback Voltage in Adjustable Mode	$V_{FB\_}$	V_{IN} = 6V to 26V, FB3 or FB5, duty factor = 20% to 80% (Note 2)	0.990	1.005	1.020	V
Output-Voltage Adjust Range		Either SMPS	1.0		5.5	V
FB3, FB5 Dual-Mode Threshold			0.1		0.2	V
Feedback Input Leakage Current		V_{FB3} = V_{FB5} = 1.1V	-0.1		+0.1	µA
DC Load Regulation		Either SMPS, $\overline{SKIP}$ = V_{CC}, I_{LOAD} = 0 to full load		-0.1		%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line-Regulation Error		Either SMPS, duty cycle = 10% to 90%			1		%
Operating Frequency (Note 1)	f_{OSC}	FSEL = GND		170	200	230	kHz
		FSEL = REF		270	300	330	
		FSEL = V_{CC}		425	500	575	
Maximum Duty Factor (Note 1)	D_{MAX}	FSEL = GND		91	93		%
		FSEL = REF		91	93		
		FSEL = V_{CC}		91	93		
Minimum On-Time	$t_{ON(MIN)}$	(Note 3)				200	ns
SMPS3 to SMPS5 Phase Shift		SMPS5 starts after SMPS3			40		%
					144		Deg
CURRENT LIMIT							
ILIM_ Adjustment Range				0.5		V_{REF}	V
Current-Sense Input Range		CSH_, CSL_		0		5.5	V
Current-Sense Input Leakage Current		CSH_, $V_{CSH\_}$ = 5.5V		-1		+1	µA
Current-Limit Threshold (Fixed)	$V_{LIMIT\_}$	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM_ = V_{CC}		70	75	80	mV
Current-Limit Threshold (Adjustable)	$V_{LIMIT\_}$	$V_{CSH\_}$ - $V_{CSL\_}$	$V_{ILIM\_}$ = 2.00V	170	200	230	mV
			$V_{ILIM\_}$ = 1.00V	91	100	109	
			$V_{ILIM\_}$ = 0.50V	42	50	58	
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = V_{CC}, percent of current limit			-120		%
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{PGND} - $V_{LX\_}$, $\overline{SKIP}$ = GND, ILIM_ = V_{CC}			3		mV
Idle-Mode™ Threshold	V_{IDLE}	$V_{CSH\_}$ - $V_{CSL\_}$	ILIM_ = V_{CC}	10	16	22	mV
			With respect to current-limit threshold (V_{LIMIT})		20		%
ILIM_ Leakage Current		ILIM3 = ILIM5 = GND or V_{CC}		-0.1		+0.1	µA
Soft-Start Ramp Time	t_{SS}	Measured from the rising edge of ON_ to full scale			512 / f_{OSC}		s
INTERNAL FIXED LINEAR REGULATORS							
LDO5 Output Voltage	V_{LDO5}	ON3 = ON5 = GND, 6V < V_{IN} < 26V, 0 < I_{LDO5} < 100mA		4.80	4.95	5.10	V
LDO5 Undervoltage-Lockout Fault Threshold		Rising edge, hysteresis = 1%		3.75	4.0	4.25	V
LDO5 Bootstrap Switch Threshold		Rising edge of CSL5, hysteresis = 1%		4.41		4.75	V
LDO5 Bootstrap Switch Resistance		LDO5 to CSL5, V_{CSL5} = 5V, I_{LDO5} = 50mA			0.75	3	Ω

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High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO3 Output Voltage	V_{LDO3}	Standby mode, 6V < V_{IN} < 26V, 0 < I_{LOAD} < 100mA	3.20	3.35	3.42	V
LDO3 Bootstrap Switch Threshold		Rising edge of CSL3, hysteresis = 1%	2.83		3.10	V
LDO3 Bootstrap Switch Resistance		LDO3 to CSL3, V_{CSL3} = 3.2V, I_{LDO3} = 50mA		1	3	Ω
Short-Circuit Current		LDO3 = LDO5 = GND, CSL3 = CSL5 = GND		150	220	mA
Short-Circuit Current (Switched Over to CSL_)		LDO3 = LDO5 = GND, V_{CSL3} > 3.1V, V_{CSL5} > 4.7V	250			mA
AUXILIARY LINEAR REGULATOR (MAX1537 ONLY)						
LDOA Voltage Range	V_{LDOA}		5		23	V
INA Voltage Range	V_{INA}		6		24	V
LDOA Regulation Threshold, Internal Feedback		ADJA = GND, 0 < I_{LDOA} < 120mA, V_{INA} > 13V	11.4	12.0	12.4	V
ADJA Regulation Threshold, External Feedback	V_{ADJA}	0 < I_{LDOA} < 120mA, V_{LDOA} > 5.0V and V_{INA} > V_{LDOA} + 1V	1.94	2.00	2.06	V
ADJA Dual-Mode Threshold			0.1	0.15	0.2	V
ADJA Leakage Current		V_{ADJA} = 2.1V	-0.1		+0.1	µA
LDOA Current Limit		V_{LDOA} forced to V_{INA} - 1V, V_{ADJA} = 1.9V, V_{INA} > 6V	150			mA
Secondary Feedback Regulation Threshold		V_{INA} - V_{LDOA}	0.65	0.8	0.95	V
DL Duty Factor		V_{INA} - V_{LDOA} < 0.7V, pulse width with respect to switching period		33		%
INA Quiescent Current	I_{INA}	V_{INA} = 24V, I_{LDOA} = no load		50	165	µA
INA Shunt Sink Current		V_{INA} = 28V	10			mA
INA Leakage Current	$I_{INA(SHDN)}$	V_{INA} = 5V, LDOA disabled			30	µA
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	1.985	2.00	2.015	V
Reference Load Regulation		I_{REF} = -10µA to +100µA	1.980		2.020	V
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 350mV		1.95		V
FAULT DETECTION						
Output Overvoltage Trip Threshold		$\overline{OVP}$ = GND, with respect to error-comparator threshold	8	11	15	%
Output Overvoltage Fault-Propagation Delay	t_{OVP}	50mV overdrive		10		µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold	65	70	75	%
Output Undervoltage Fault-Propagation Delay	t_{UVP}	50mV overdrive		10		µs
Output Undervoltage-Protection Blanking Time	t_{BLANK}	From rising edge of ON_		6144 / f_{OSC}		s
PGOOD Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%	-14	-10	-7.5	%
PGOOD Propagation Delay	$t_{PGOOD\_}$	Falling edge, 50mV overdrive		10		µs
PGOOD Output Low Voltage		I_{SINK} = 4mA			0.4	V
PGOOD Leakage Current	$I_{PGOOD\_}$	High state, PGOOD forced to 5.5V			1	µA
PGDLY Pullup Current		PGDLY = GND	4	5	6	µA
PGDLY Pulldown Resistance				10	25	Ω
PGDLY Trip Threshold			REF-0.2	REF	REF+0.2	V
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C		+160		°C
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V		1.5	5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state		1.7	5	Ω
		DL_, low state		0.6	3	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V		2		A
DL_ Gate-Driver Source Current	I_{DL}	DL_ forced to 2.5V		1.7		A
DL_ Gate-Driver Sink Current	$I_{DL\ (SINK)}$	DL_ forced to 2.5V		3.3		A
Dead Time	t_{DEAD}	DL_ rising		35		ns
		DH_ rising		26		
LX_, BST_ Leakage Current		$V_{BST\_}$ = $V_{LX\_}$ = 26V		<2	20	µA
INPUTS AND OUTPUTS						
Logic Input Voltage		$\overline{SKIP}$, hysteresis = 600mV, High	2.4			V
		$\overline{SKIP}$, hysteresis = 600mV, Low			0.8	
Fault Enable Logic Input Voltage		$\overline{OVP}$, $\overline{UVP}$, ONA, High	0.7 x V_{CC}			V
		$\overline{OVP}$, $\overline{UVP}$, ONA, Low			0.4	
Logic Input Current		$\overline{OVP}$, $\overline{UVP}$, $\overline{SKIP}$, ONA	-1		+1	µA
$\overline{SHDN}$ Input Trip Level		Rising trip level	1.10	1.6	2.20	V
		Falling trip level	0.96	1	1.04	
ON_ Input Voltage		Clear fault level/SMPS off level			0.8	V
		Delay start level (REF)	1.9		2.1	
		SMPS on level	2.4			

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FSEL Three-Level Input Logic		High	V_{CC} - 0.2			V
		REF	1.7		2.3	
		GND			0.4	
Input Leakage Current		$\overline{OVP}$, $\overline{UVP}$, $\overline{SKIP}$, ONA, ON3, ON5 = GND or V_{CC}	-1		+1	µA
		$\overline{SHDN}$, 0V or 26V	-1		+1	
		FSEL = GND or V_{CC}	-3		+3	
CSL_ Discharge-Mode On-Resistance	$R_{DISCHARGE}$			10	25	Ω
CSL_ Synchronous-Rectifier Discharge-Mode Turn-On Level			0.2	0.3	0.4	V

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
INPUT SUPPLIES (Note 1)					
V_{IN} Input Voltage Range	V_{IN}	LDO5 in regulation	6	26	V
		IN = LDO5, V_{OUT5} < 4.4V	4.5	5.5	
V_{IN} Operating Supply Current	I_{IN}	LDO5 switched over to CSL5, either SMPS on		35	µA
V_{IN} Standby Supply Current	$I_{IN(STBY)}$	V_{IN} = 6V to 26V, both SMPS off, includes $I_{\overline{SHDN}}$		170	µA
V_{IN} Shutdown Supply Current	$I_{IN(SHDN)}$	V_{IN} = 6V to 26V		17	µA
Quiescent Power Consumption	P_Q	Both SMPS on, FB3 = FB5 = $\overline{SKIP}$ = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V, V_{INA} = 15V, I_{LDOA} = 0, P_{IN} + P_{CSL3} + P_{CSL5} + P_{INA}		4.5	mW
V_{CC} Quiescent Supply Current	I_{CC}	Both SMPS on, FB3 = FB5 = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V		2.5	mA
MAIN SMPS CONTROLLERS					
3.3V Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)	3.28	3.38	V
5V Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)	4.975	5.125	V
Feedback Voltage in Adjustable Mode	V_{FB3}, V_{FB5}	V_{IN} = 6V to 26V, FB3 or FB5, duty factor = 20% to 80% (Note 2)	0.982	1.018	V
Output-Voltage Adjust Range		Either SMPS	1.0	5.5	V
FB3, FB5 Adjustable-Mode Threshold Voltage		Dual-mode comparator	0.1	0.2	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Operating Frequency (Note 1)	f_{OSC}	FSEL = GND		170	230	kHz
		FSEL = REF		240	330	
		FSEL = V_{CC}		375	575	
Maximum Duty Factor (Note 1)	D_{MAX}	FSEL = GND		91		%
		FSEL = REF		91		
		FSEL = V_{CC}		91		
Minimum On-Time	$t_{ON(MIN)}$				250	ns
CURRENT LIMIT						
ILIM_ Adjustment Range				0.5	V_{REF}	V
Current-Limit Threshold (Fixed)	$V_{LIMIT\_}$	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM_ = V_{CC}		67	83	mV
Current-Limit Threshold (Adjustable)	$V_{LIMIT\_}$	$V_{CSH\_}$ - $V_{CSL\_}$	$V_{ILIM\_}$ = 2.00V	170	230	mV
			$V_{ILIM\_}$ = 1.00V	90	110	
			$V_{ILIM\_}$ = 0.50V	40	60	
INTERNAL FIXED LINEAR REGULATORS						
LDO5 Output Voltage	V_{LDO5}	ON3 = ON5 = GND, 6V < V_{IN} < 26V, 0 < I_{LDO5} < 100mA		4.8	5.1	V
LDO5 Undervoltage-Lockout Fault Threshold		Rising edge, hysteresis = 1%		3.75	4.30	V
LDO3 Output Voltage	V_{LDO3}	Standby mode, 6V < V_{IN} < 28V, 0 < I_{LOAD} < 100mA		3.20	3.43	V
AUXILIARY LINEAR REGULATOR (MAX1537 ONLY)						
LDOA Voltage Range	V_{LODA}			5	23	V
INA Voltage Range	V_{INA}			6	24	V
LDOA Regulation Threshold, Internal Feedback		ADJA = GND, 0 < I_{LDOA} < 120mA, V_{INA} > 13V		11.40	12.55	V
ADJA Regulation Threshold, External Feedback	V_{ADJA}	0 < I_{LDOA} < 120mA, V_{LDOA} > 5.0V and V_{INA} > V_{LDOA} + 1V		1.94	2.08	V
ADJA Dual-Mode Threshold		ADJA		0.10	0.25	V
Secondary Feedback Regulation Threshold		V_{INA} - V_{LDOA}		0.63	0.97	V
INA Quiescent Current	I_{INA}	V_{INA} = 24V, I_{LDOA} = no load			165	µA
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.97	2.03	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, V_{CC} = 5V, FSEL = REF, $\overline{SKIP}$ = GND, $V_{ILIM\_}$ = V_{LDO5}, V_{INA} = 15V, V_{LDOA} = 12V, I_{LDO5} = I_{LDO3} = I_{LDOA} = no load, $\mathbf{T_A}$ **= -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
FAULT DETECTION						
Output Overvoltage Trip Threshold		$\overline{OVP}$ = GND, with respect to error-comparator threshold		+8	+15	%
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold		+65	+75	%
PGOOD Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		-14.0	-7.0	%
PGOOD Output Low Voltage		I_{SINK} = 4mA			0.4	V
PGDLY Pulldown Resistance					25	Ω
PGDLY Trip Threshold				REF-0.2	REF+0.2	V
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V			5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			5	Ω
		DL_, low state			3	
INPUTS AND OUTPUTS						
Logic Input Voltage		$\overline{SKIP}$, hysteresis = 600mV	High	2.4		V
			Low		0.8	
Fault Enable Logic Input Voltage		$\overline{OVP}$, $\overline{UVP}$, ONA	High	0.7 x V_{CC}		V
			Low		0.4	
$\overline{SHDN}$ Input Trip Level		Rising trip level		1.1	2.2	V
		Falling trip level		0.95	1.05	
ON_ Input Voltage		Clear fault level			0.8	V
		SMPS off level			1.6	
		Delay start level (REF)		1.9	2.1	
		SMPS on level		2.4		
FSEL Three-Level Input Logic		High		V_{CC} - 0.2		V
		REF		1.7	2.3	
		GND			0.4	

Note 1: The MAX1533/MAX1537 cannot operate over all combinations of frequency, input voltage (V_{IN}), and output voltage. For large input-to-output differentials and high-switching frequency settings, the required on-time may be too short to maintain the regulation specifications. Under these conditions, a lower operating frequency must be selected. The minimum on-time must be greater than 150ns, regardless of the selected switching frequency. On-time and off-time specifications are measured from 50% point to 50% point at the DH_ pin with LX_ = GND, $V_{BST\_}$ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 2: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage has a DC regulation level higher than the trip level by approximately 1% due to slope compensation.

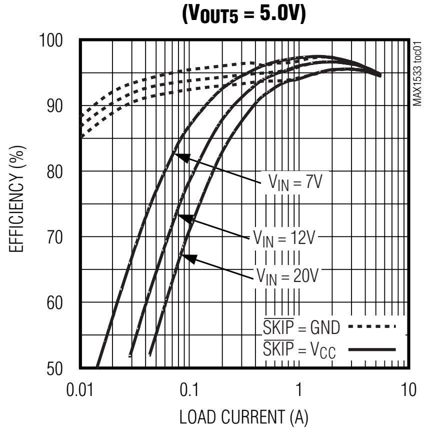
Note 3: Specifications are guaranteed by design, not production tested.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

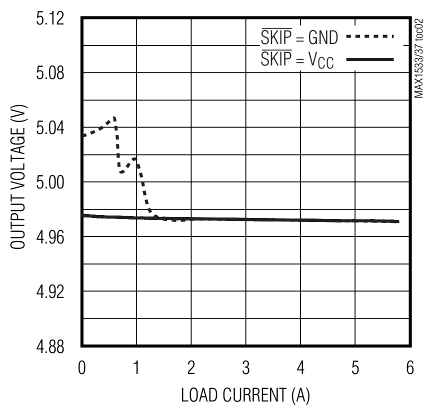
Typical Operating Characteristics

(MAX1537 circuit of Figure 1, V_{IN} = 12V, LDO5 = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

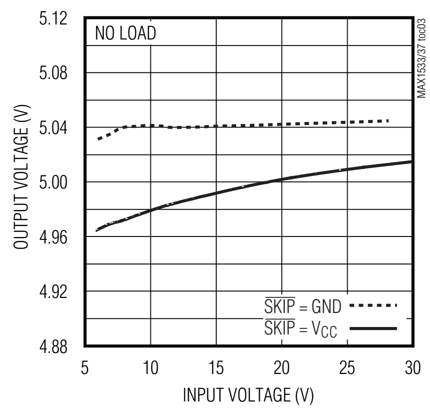
PWM5 EFFICIENCY vs. LOAD CURRENT (V_{OUT5} = 5.0V)



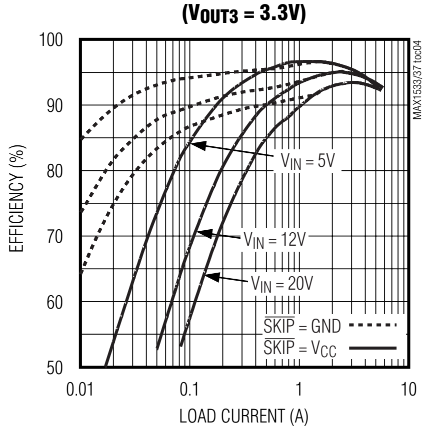
5V OUTPUT VOLTAGE (OUT5) vs. LOAD CURRENT



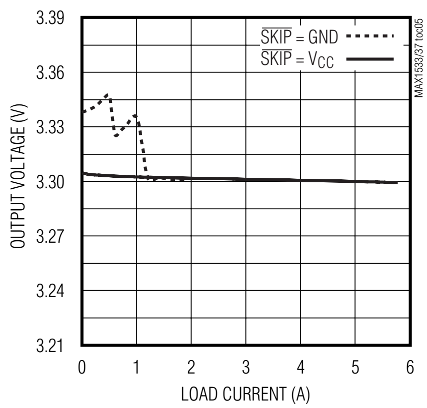
5V OUTPUT VOLTAGE (OUT5) vs. INPUT VOLTAGE



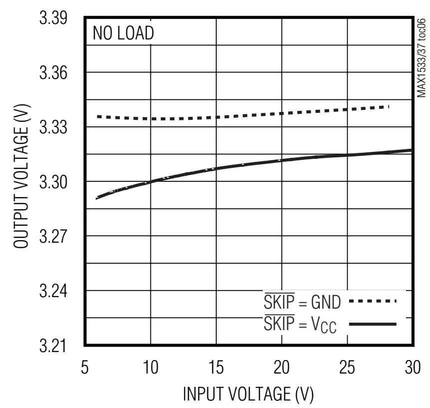
PWM3 EFFICIENCY vs. LOAD CURRENT (V_{OUT3} = 3.3V)



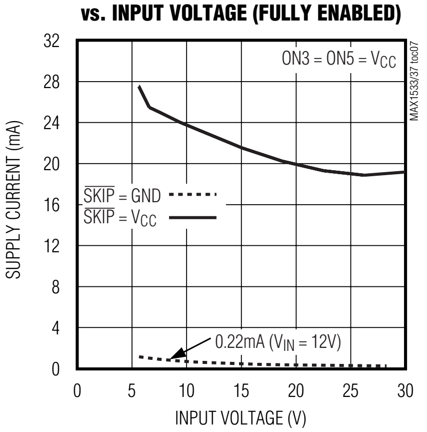
3.3V OUTPUT VOLTAGE (OUT3) vs. LOAD CURRENT



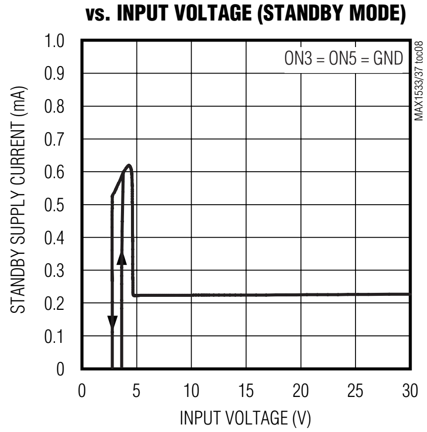
3.3V OUTPUT VOLTAGE (OUT3) vs. INPUT VOLTAGE



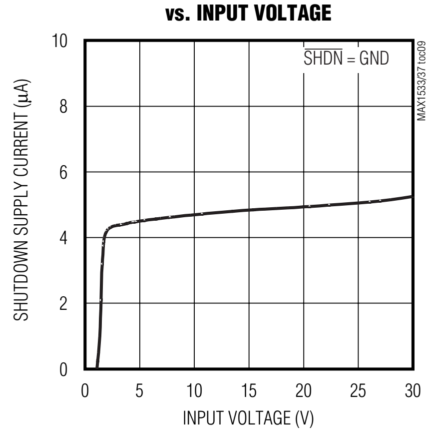
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FULLY ENABLED)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (STANDBY MODE)



SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE

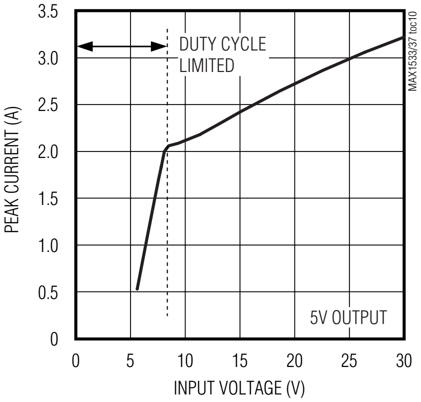


High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

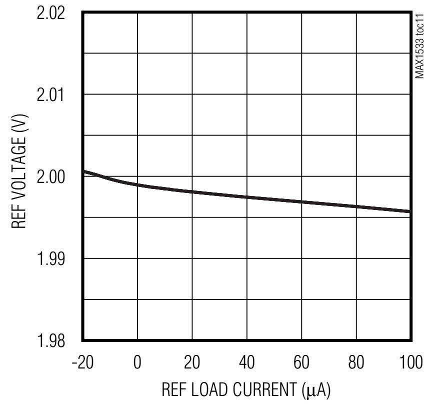
Typical Operating Characteristics (continued)

(MAX1537 circuit of Figure 1, V_{IN} = 12V, LDO5 = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

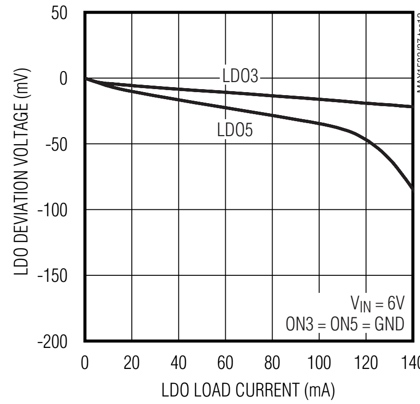
IDLE-MODE CURRENT vs. INPUT VOLTAGE



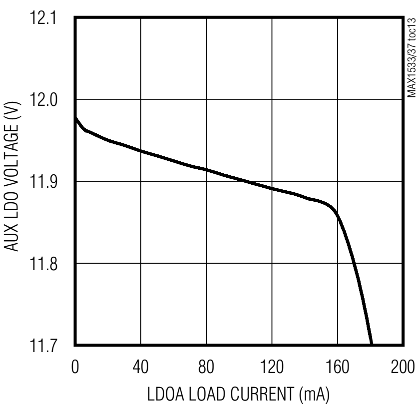
2.0V REFERENCE LOAD REGULATION



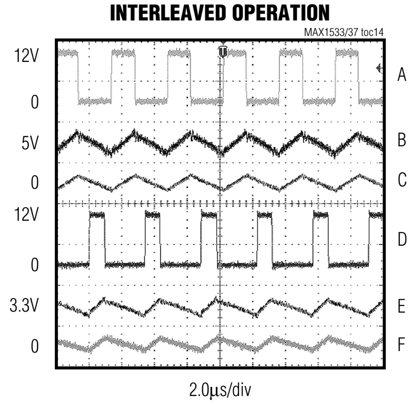
LINEAR-REGULATOR LOAD REGULATION



AUXILIARY LINEAR-REGULATOR LOAD REGULATION

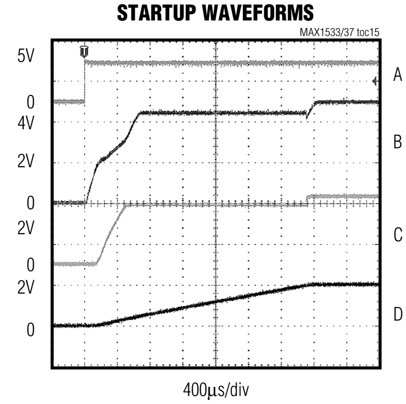


INTERLEAVED OPERATION



A. LX5, 10V/div
B. 5V OUTPUT, 100mV/div
C. PWM5 INDUCTOR CURRENT, 5A/div
D. LX3, 10V/div
E. 3.3V OUTPUT, 100mV/div
F. PWM3 INDUCTOR CURRENT, 5A/div

LINEAR-REGULATOR STARTUP WAVEFORMS

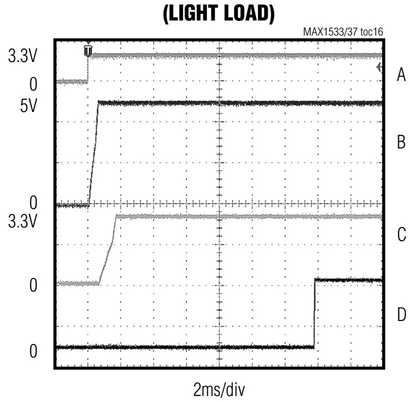


A. $\overline{SHDN}$, 5V/div
B. LDO5, 2V/div
C. LDO3, 2V/div
D. REF, 2V/div
100Ω LOAD ON LDO5 AND LDO3

Typical Operating Characteristics (continued)

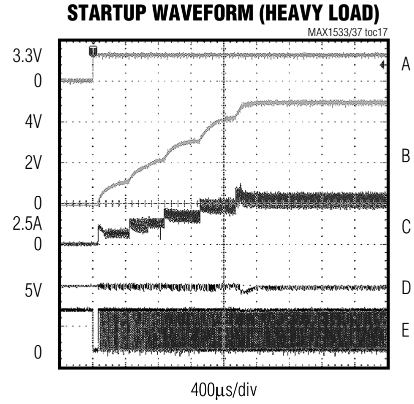
(MAX1537 circuit of Figure 1, V_{IN} = 12V, LDO5 = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

DELAYED STARTUP WAVEFORM (LIGHT LOAD)



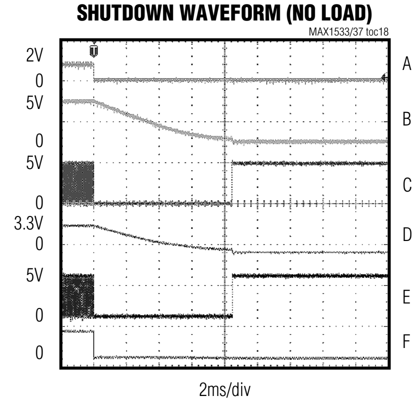
A. ON5, 5V/div
B. 5V OUTPUT, 2V/div
C. 3.3V OUPUT, 2V/div
D. PGOOD, 2V/div
100Ω LOAD ON OUT5 AND OUT3, ON3 = REF

STARTUP WAVEFORM (HEAVY LOAD)



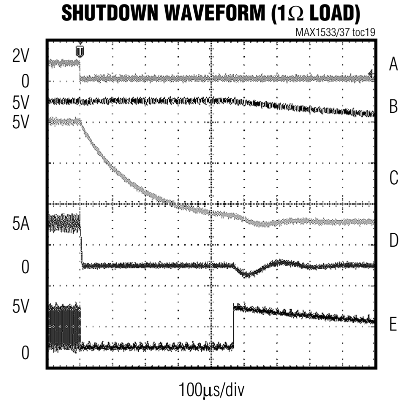
A. ON5, 5V/div
B. 5V OUTPUT, 2V/div
C. INDUCTOR CURRENT, 5A/div
D. LDO5, 1V/div
E. DL5, 5V/div
1.0Ω LOAD

SHUTDOWN WAVEFORM (NO LOAD)



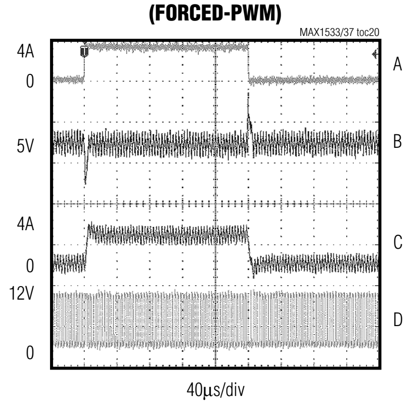
A. $\overline{SHDN}$, 5V/div
B. 5V OUTPUT, 5V/div
C. DL5, 5V/div
D. 3.3V OUTPUT, 5V/div
E. DL3, 5V/div
F. PGOOD, 5V/div
ON3 = ON5 = V_{CC}, $\overline{OVP}$ = GND

SHUTDOWN WAVEFORM (1Ω LOAD)



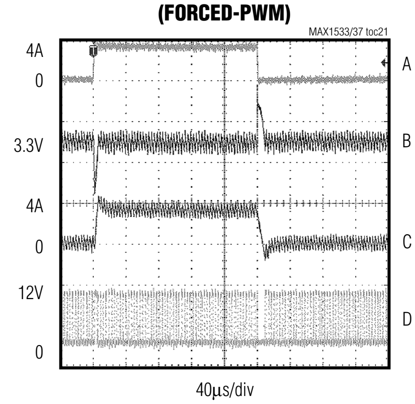
A. $\overline{SHDN}$, 5V/div
B. LDO5, 2V/div
C. 5V OUTPUT, 2V/div
D. INDUCTOR CURRENT, 5A/div
E. DL5, 5V/div
ON3 = ON5 = V_{CC}, $\overline{OVP}$ = GND

5V OUTPUT LOAD TRANSIENT (FORCED-PWM)



A. I_{OUT5} = 0.2A TO 4A, 5A/div
B. V_{OUT5} = 5.0V, 100mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX5, 10V/div
$\overline{SKIP}$ = V_{CC}

3.3V OUTPUT LOAD TRANSIENT (FORCED-PWM)



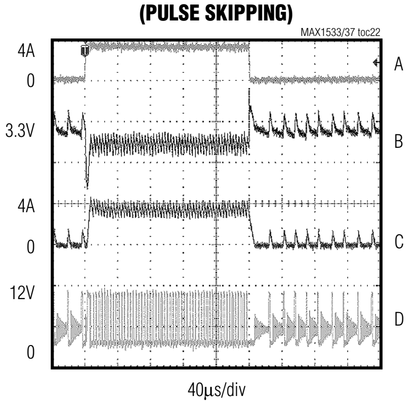
A. I_{OUT3} = 0.2A TO 4A, 5A/div
B. V_{OUT3} = 3.3V, 100mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX3, 10V/div
$\overline{SKIP}$ = V_{CC}

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics (continued)

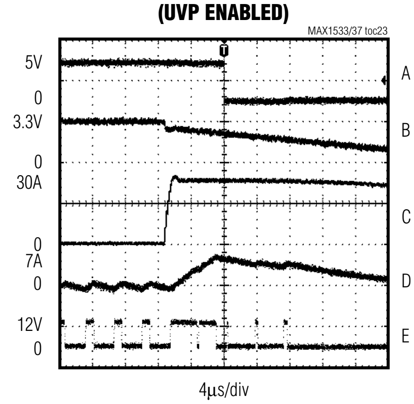
(MAX1537 circuit of Figure 1, V_{IN} = 12V, LDO5 = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

3.3V OUTPUT LOAD TRANSIENT (PULSE SKIPPING)



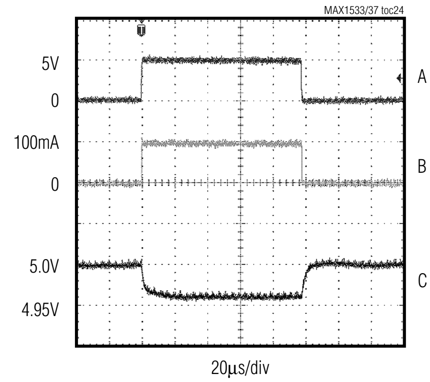
A. I_{OUT3} = 0.2A TO 4A, 5A/div
B. V_{OUT3} = 3.3V, 100mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX3, 10V/div
$\overline{SKIP}$ = GND

OUTPUT OVERLOAD (UVP ENABLED)



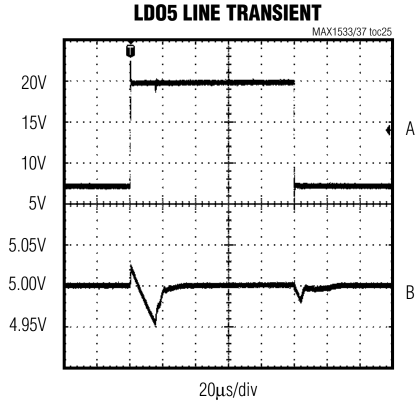
A. PGOOD2, 5V/div
B. 3.3V OUTPUT, 3.3V/div
C. LOAD (0 TO 30A), 20A/div
D. INDUCTOR CURRENT, 10A/div
E. LX3, 20V/div

LDO5 LOAD TRANSIENT



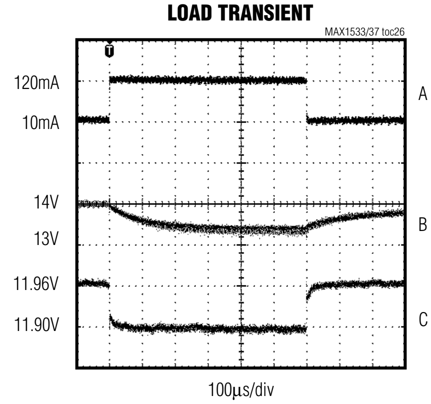
A. CONTROL SIGNAL, 5V/div
B. I_{LDO5} = 1mA TO 100mA, 100mA/div
C. LDO5, 50m/div
ON3 = ON5 = GND

LDO5 LINE TRANSIENT



A. INPUT VOLTAGE (V_{IN} = 7V TO 20V), 5V/div
B. LDO5 OUTPUT VOLTAGE, 50mV/div
ON3 = ON5 = GND, I_{LDO5} = 20mA

AUXILIARY LINEAR-REGULATOR LOAD TRANSIENT



A. I_{LDOA} = 10mA TO 100mA, 100mA/div
B. INA, 1V/div
C. LDOA, 50mV/div
INA = VOLTAGE GENERATED BY SECONDARY TRANSFORMER WINDING

Pin Description

PIN		NAME	FUNCTION
MAX1533	MAX1537		
—	1	ADJA	Auxiliary Feedback Input. Connect a resistive voltage-divider from LDOA to analog ground to adjust the auxiliary linear-regulator output voltage. ADJA regulates at 2V. Connect ADJA to GND for nominal 12V output using internal feedback.
1	2	ON5	5V SMPS Enable Input. The 5V SMPS is enabled if ON5 is greater than the SMPS on level and disabled if ON5 is less than the SMPS off level. If ON5 is connected to REF, the 5V SMPS starts after the 3.3V SMPS reaches regulation (delay start). Drive ON5 below the clear fault level to reset the fault latches.
2	3	ON3	3.3V SMPS Enable Input. The 3.3V SMPS is enabled if ON3 is greater than the SMPS on level and disabled if ON3 is less than the SMPS off level. If ON3 is connected to REF, the 3.3V SMPS starts after the 5V SMPS reaches regulation (delay start). Drive ON3 below the clear fault level to reset the fault latches.
—	4	ONA	LDOA Enable Input. When ONA is low, LDOA is high impedance and the secondary winding control is off. When ONA is high, LDOA is on. Connect to LDO3, LDO5, CSL3, CSL5, or other output for desired automatic startup sequencing.
3	5	FSEL	Frequency-Select Input. This three-level logic input sets the controller's switching frequency. Connect to GND, REF, or V_{CC} to select the following typical switching frequencies: V_{CC} = 500kHz, REF = 300kHz, GND = 200kHz
4	6	ILIM3	3.3V SMPS Peak Current-Limit Threshold Adjustment. The current-limit threshold defaults to 75mV if ILIM3 is connected to V_{CC}. In adjustable mode, the current-limit threshold across CSH3 and CSL3 is precisely 1/10th the voltage seen at ILIM3 over a 500mV to 2.0V range. The logic threshold for switchover to the 75mV default value is approximately V_{CC} - 1V.
5	7	ILIM5	5V SMPS Peak Current-Limit Threshold. The current-limit threshold defaults to 75mV if ILIM5 is connected to V_{CC}. In adjustable mode, the current-limit threshold across CSH5 and CSL5 is precisely 1/10th the voltage seen at ILIM5 over a 500mV to 2.0V range. The logic threshold for switchover to the 75mV default value is approximately V_{CC} - 1V.
6	8	REF	2.0V Reference Voltage Output. Bypass REF to analog ground with a 0.1µF or greater ceramic capacitor. The reference can source up to 100µA for external loads. Loading REF degrades output-voltage accuracy according to the REF load-regulation error. The reference shuts down when $\overline{SHDN}$ is low.
7	9	GND	Analog Ground. Connect the backside pad to GND.
8	10	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 20Ω resistor. Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.
9	11	PGDLY	Power-Good One-Shot Delay. Place a timing capacitor on PGDLY to delay PGOOD going high. PGDLY has a 5µA pullup current and a 10Ω pulldown. The pulldown is activated when power is not good. When power is good, the pulldown is shut off and the 5µA pullup is activated. When PGDLY crosses REF, PGOOD is enabled.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1533	MAX1537		
10	12	PGOOD	Open-Drain Power-Good Output. PGOOD is low if either output is more than 10% (typ) below the normal regulation point, during soft-start, and in shutdown. PGOOD is delayed on the rising edge by the PGDLY one-shot timer. PGOOD becomes high impedance when both SMPS outputs are in regulation.
11	13	$\overline{UVP}$	Undervoltage Fault-Protection Control. Connect $\overline{UVP}$ to GND to select the default overvoltage threshold of 70% of nominal. Connect to V_{CC} to disable undervoltage protection and clear the undervoltage fault latch.
12	14	DH3	High-Side Gate-Driver Output for 3.3V SMPS. DH3 swings from LX3 to BST3.
13	15	BST3	Boost Flying-Capacitor Connection for 3.3V SMPS. Connect to an external capacitor and diode as shown in Figure 6. An optional resistor in series with BST3 allows the DH3 pullup current to be adjusted.
14	16	LX3	Inductor Connection for 3.3V SMPS. Connect LX3 to the switched side of the inductor. LX3 serves as the lower supply rail for the DH3 high-side gate driver.
15	17	$\overline{OVP}$	Overvoltage Fault-Protection Control. Connect $\overline{OVP}$ to GND to select the default overvoltage threshold of +11% above nominal. Connect to V_{CC} to disable overvoltage protection and clear the overvoltage fault latch.
16	18	CSH3	Positive Current-Sense Input for 3.3V SMPS. Connect to the positive terminal of the current-sense element. Figure 9 describes two different current-sensing options.
17	19	CSL3	Negative Current-Sense Input for 3.3V SMPS. Connect to the negative terminal of the current-sense element. Figure 9 describes two different current-sensing options. CSL3 also serves as the bootstrap input for LDO3.
18	20	FB3	Feedback Input for 3.3V SMPS. Connect to GND for fixed 3.3V output. In adjustable mode, FB3 regulates to 1V.
19	21	LDO3	3.3V Internal Linear-Regulator Output. Bypass with 2.2µF (min) (1µF/20mA). Provides 100mA (min). Power is taken from LDO5. If CSL3 is greater than 3V, the linear regulator shuts down and LDO3 connects to CSL3 through a 1Ω switch rated for loads up to 200mA.
20	22	DL3	Low-Side Gate-Driver Output for 3.3V SMPS. DL3 swings from PGND to LDO5.
21	23	PGND	Power Ground
22	24	DL5	Low-Side Gate-Driver Output for 5V SMPS. DL5 swings from PGND to LDO5.
23	25	LDO5	5V Internal Linear-Regulator Output. Bypass with 2.2µF (min) (1µF/20mA). Provides power for the DL_ low-side gate drivers, the DH_ high-side drivers through the BST diodes, the PWM controller, logic, and reference through the V_{CC} pin, as well as the LDO3 internal 3.3V linear regulator. Provides 100mA (min) for external loads (+25mA for gate drivers). If CSL5 is greater than 4.5V, the linear regulator shuts down and LDO5 connects to CSL5 through a 0.75Ω switch rated for loads up to 200mA.
24	26	FB5	Feedback Input for 5V SMPS. Connect to GND for fixed 5V output. In adjustable mode, FB5 regulates to 1V.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1533	MAX1537		
25	27	CSL5	Negative Current-Sense Input for 5V SMPS. Connect to the negative terminal of the current-sense element. Figure 9 describes two different current-sensing options. CSL5 also serves as the bootstrap input for LDO5.
26	28	CSH5	Positive Current-Sense Input for 5V SMPS. Connect to the positive terminal of the current-sense element. Figure 9 describes two different current-sensing options.
27	29	IN	Input of the Startup Circuitry and the LDO5 Internal 5V Linear Regulator. Bypass to PGND with 0.22µF close to the IC.
28	30	LX5	Inductor Connection for 5V SMPS. Connect LX5 to the switched side of the inductor. LX5 serves as the lower supply rail for the DH5 high-side gate driver.
29	31	BST5	Boost Flying-Capacitor Connection for 5V SMPS. Connect to an external capacitor and diode as shown in Figure 6. An optional resistor in series with BST5 allows the DH5 pullup current to be adjusted.
30	32	DH5	High-Side Gate-Driver Output for 5V SMPS. DH5 swings from LX5 to BST5.
31	33	$\overline{\text{SKIP}}$	Pulse-Skipping Control Input. Connect to V_{CC} for low-noise forced-PWM mode. Connect to GND for high-efficiency pulse-skipping mode at light loads.
32	34	$\overline{\text{SHDN}}$	Shutdown Control Input. The device enters its 5µA supply-current shutdown mode if $V_{\overline{SHDN}}$ is less than the $\overline{\text{SHDN}}$ input falling-edge trip level and does not restart until $V_{\overline{SHDN}}$ is greater than the $\overline{\text{SHDN}}$ input rising-edge trip level. Connect $\overline{\text{SHDN}}$ to V_{IN} for automatic startup. $\overline{\text{SHDN}}$ can be connected to V_{IN} through a resistive voltage-divider to implement a programmable undervoltage lockout.
—	35	INA	Supply Voltage Input for the Auxiliary LDOA Linear Regulator. INA is clamped with an internal shunt to 26V.
—	36	LDOA	Adjustable (12V Nominal) 150mA Auxiliary Linear-Regulator Output. Input supply comes from INA. Bypass LDOA to GND with 2.2µF (min) (1µF/20mA). Secondary feedback threshold is set at INA - LDOA = 0.8V, and triggers the DL5 on the 5V SMPS only. ONA high enables regulator output and secondary regulation. PGOOD is not affected by the state of LDOA.

Table 1. Component Selection for Standard Applications

COMPONENT	5A/300kHz	5A/500kHz
Input Voltage	V_{IN} = 7V to 24V	V_{IN} = 7V to 24V
$C_{IN\_}$, Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM
C_{OUT5}, Output Capacitor	150µF, 6.3V, 40mΩ, low-ESR capacitor Sanyo 6TPB150ML	150µF, 6.3V, 40mΩ, low-ESR capacitor Sanyo 6TPB150ML
C_{OUT3}, Output Capacitor	220µF, 4V, 40mΩ, low-ESR capacitor Sanyo 4TPB220ML	220µF, 4V, 40mΩ, low-ESR capacitor Sanyo 4TPB220ML
$N_{H\_}$ High-Side MOSFET	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V
$N_{L\_}$ Low-Side MOSFET	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1
$D_{L\_}$ Schottky Rectifier (if needed)	2A, 30V, 0.45V_f Nihon EC21QS03L	2A, 30V, 0.45V_f Nihon EC21QS03L
Inductor/Transformer	T1 = 6.8µH, 1:2 turns Sumida 4749-T132 L1 = 5.8µH, 8.6A Sumida CDRH127-5R8NC	3.9µH Sumida CDRH124-3R9NC
R_{CS}	10mΩ ±1%, 0.5W resistor IRC LR2010-01-R010F or Dale WSL-2010-R010F	10mΩ ±1%, 0.5W resistor IRC LR2010-01-R010F or Dale WSL-2010-R010F

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX	www.avx.com
Central Semiconductor	www.centralsemi.com
Coilcraft	www.coilcraft.com
Coiltronics	www.coiltronics.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
Kemet	www.kemet.com

SUPPLIER	WEBSITE
Panasonic	www.panasonic.com/industrial
Sanyo	www.secc.co.jp
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com

Detailed Description

The MAX1533/MAX1537 standard application circuit (Figure 1) generates the 5V/5A and 3.3V/5A typical of the main supplies in a notebook computer. The input supply range is 7V to 24V. See Table 1 for component selections and Table 2 for component manufacturers.

The MAX1533/MAX1537 contain two interleaved fixed-frequency step-down controllers designed for low-voltage power supplies. The optimal interleaved architecture guarantees out-of-phase operation, reducing the input capacitor ripple. Two internal LDOs generate the keep-alive 5V and 3.3V power. The MAX1537 has an auxiliary LDO that can be configured to the preset 12V output or an adjustable output.

Fixed Linear Regulators (LDO5 and LDO3)

Two internal linear regulators produce preset 5V (LDO5) and 3.3V (LDO3) low-power outputs. LDO5 powers LDO3, the gate drivers for the external MOSFETs, and provides the bias supply (V_{CC}) required for the SMPS analog control, reference, and logic blocks. LDO5 supplies at least 100mA for external and internal loads, including the MOSFET gate drive, which typically varies from 5mA to 50mA, depending on the switching frequency and external MOSFETs selected. LDO3 also supplies at least 100mA for external loads. Bypass LDO5 and LDO3 with a 2.2µF or greater output capacitor, using an additional 1.0µF per 20mA of internal and external load.

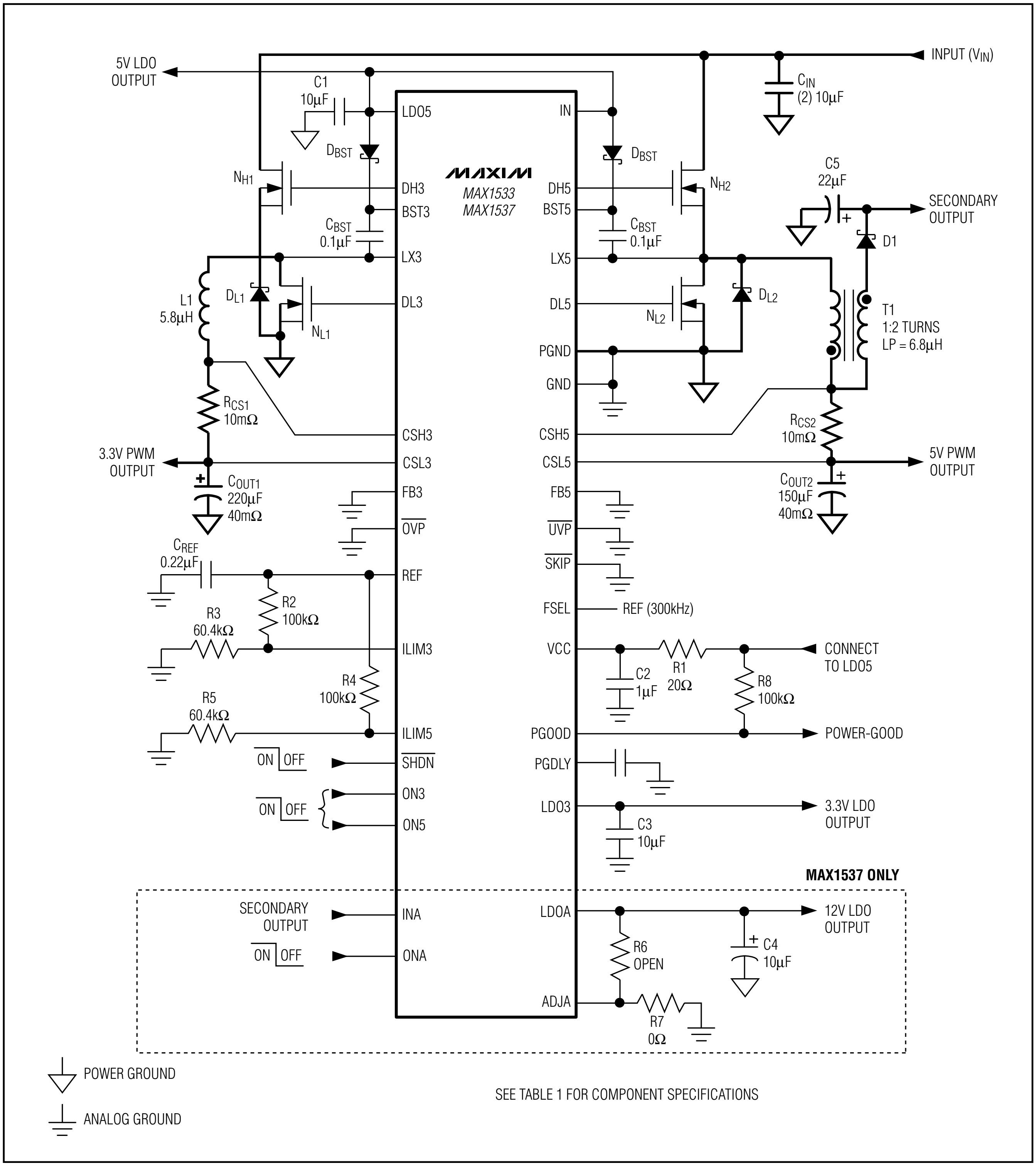


Figure 1. MAX1533/MAX1537 Standard Application Circuit

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

SMPS to LDO Bootstrap Switchover

When the 5V main output voltage is above the LDO5 bootstrap-switchover threshold, an internal 0.75Ω (typ) p-channel MOSFET shorts CSL5 to LDO5 while simultaneously shutting down the LDO5 linear regulator. Similarly, when the 3.3V main output voltage is above the LDO3 bootstrap-switchover threshold, an internal 1Ω (typ) p-channel MOSFET shorts CSL3 to LDO3 while simultaneously shutting down the LDO3 linear regulator. These actions bootstrap the device, powering the internal circuitry and external loads from the output SMPS voltages, rather than through linear regulators from the battery. Bootstrapping reduces power dissipation due to gate charge and quiescent losses by providing power from a 90%-efficient switch-mode source, rather than from a much-less-efficient linear regulator. The output current limit increases to 200mA when the LDO_ outputs are switched over.

SMPS 5V Bias Supply (LDO5 and V_{CC})

The A switch-mode power supplies (SMPS) require a 5V bias supply in addition to the high-power input supply (battery or AC adapter). This 5V bias supply is generated by the MAX1533/MAX1537s' internal 5V linear regulator (LDO5). This bootstrapped LDO allows the MAX1533/MAX1537 to power-up independently. The gate-driver input supply is connected to the fixed 5V linear-regulator output (LDO5). Therefore, the 5V LDO supply must provide V_{CC} (PWM controller) and the gate-drive power, so the maximum supply current required is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 5mA \text{ to } 50mA \text{ (typ)}$$

where I_{CC} is 1mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

Reference (REF)

The 2V reference is accurate to ±1% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.22µF or greater ceramic capacitor. The reference sources up to 100µA and sinks 10µA to support external loads. If highly accurate specifications (±0.5%) are required for the main SMPS output voltages, the reference should not be loaded. Loading the reference reduces the LDO5, LDO3, OUT5, and OUT3 output voltages slightly because of the reference load-regulation error.

System Enable/Shutdown ($\overline{SHDN}$)

Drive $\overline{SHDN}$ below the precise $\overline{SHDN}$ input falling-edge trip level to place the MAX1533/MAX1537 in their low-power shutdown state. The MAX1533/MAX1537 consume only 5µA of quiescent current while in shutdown mode. When shutdown mode activates, the reference turns off, making the threshold to exit shutdown less accurate. To guarantee startup, drive $\overline{SHDN}$ above 2.2V ($\overline{SHDN}$ input rising-edge trip level). For automatic shutdown and startup, connect $\overline{SHDN}$ to V_{IN}. The accurate 1V falling-edge threshold on $\overline{SHDN}$ can be used to detect a specific input-voltage level and shut the device down. Once in shutdown, the 1.6V rising-edge threshold activates, providing sufficient hysteresis for most applications.

SMPS Detailed Description

SMPS POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 1V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. The POR circuit also ensures that the low-side drivers are pulled low if OVP is disabled ($\overline{OVP}$ = V_{CC}), or driven high if OVP is enabled ($\overline{OVP}$ = GND) until the SMPS controllers are activated.

The V_{CC} input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (LDO5) is below the 4V input UVLO threshold. Once the 5V bias supply (LDO5) rises above this input UVLO threshold and the controllers are enabled, the SMPS controllers start switching and the output voltages begin to ramp up using soft-start.

The internal digital soft-start gradually increases the internal current-limit level during startup to reduce the input surge currents. The MAX1533/MAX1537 divide the soft-start period into five phases. During the first phase, each controller limits its current limit to only 20% of its full current limit. If the output does not reach regulation within 128 clock cycles (1 / f_{OSC}), soft-start enters the second phase and the current limit is increased by another 20%. This process repeats until the maximum current limit is reached after 512 clock cycles (1 / f_{OSC}) or when the output reaches the nominal regulation voltage, whichever occurs first (see the startup waveforms in the *Typical Operating Characteristics*).

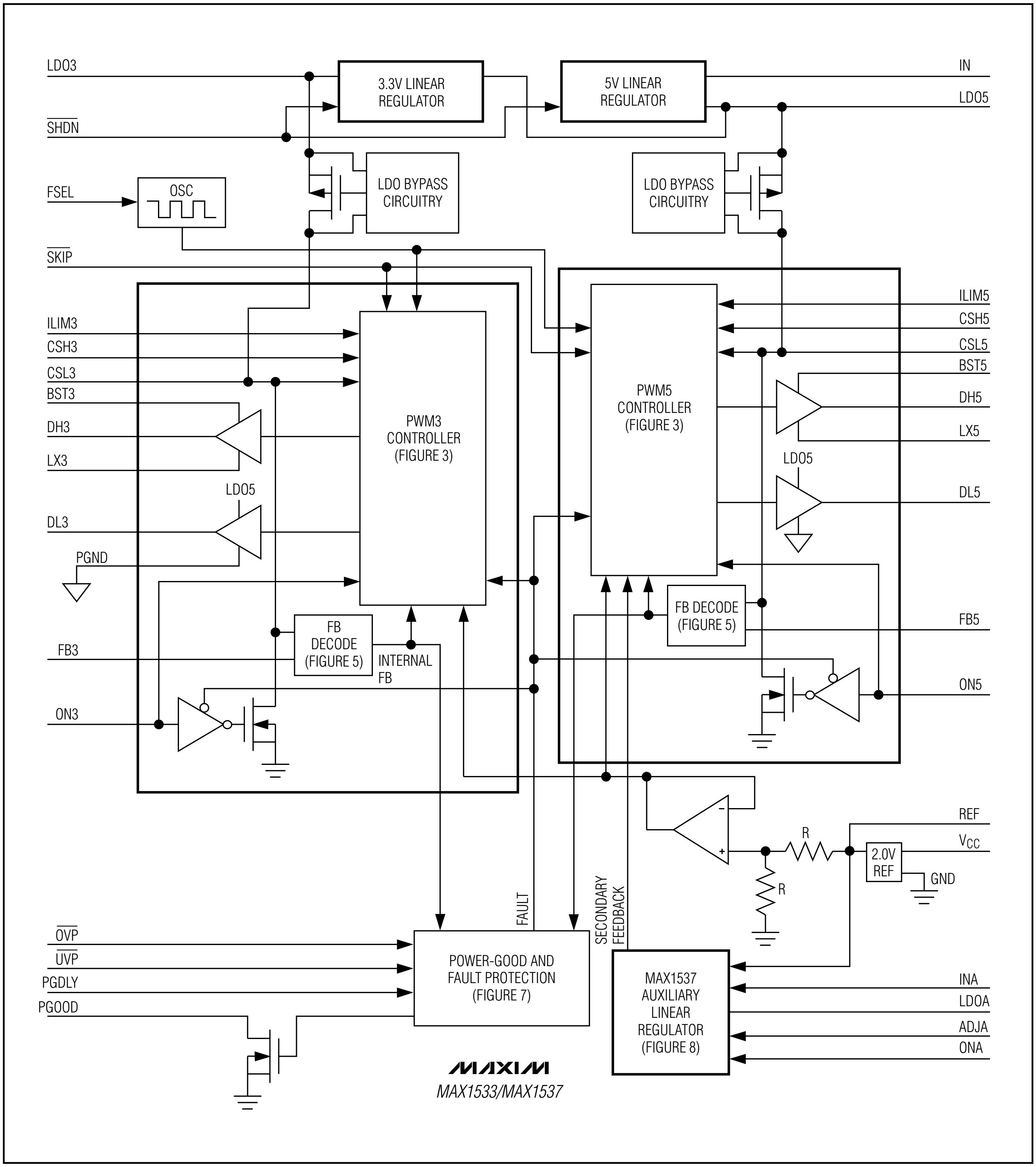


Figure 2. MAX1533/MAX1537 Functional Diagram

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

Table 3. Operating Modes

MODE	INPUTS*			OUTPUTS			
	$\overline{SHDN}$	ON5	ON3	LDO5	LDO3	5V SMPS	3V SMPS
Shutdown Mode	LOW	X	X	OFF	OFF	OFF	OFF
Standby Mode	HIGH	LOW	LOW	ON	ON	OFF	OFF
Normal Operation	HIGH	HIGH	HIGH	ON	ON	ON	ON
3.3V SMPS Active	HIGH	LOW	HIGH	ON	ON	OFF	ON
5V SMPS Active	HIGH	HIGH	LOW	ON	ON	ON	OFF
Normal Operation (Delayed 5V SMPS Startup)	HIGH	REF	HIGH	ON	ON	ON Power-up after 3.3V SMPS is in regulation	ON
Normal Operation (Delayed 3.3V SMPS Startup)	HIGH	HIGH	REF	ON	ON	ON	ON Power-up after 5V SMPS is in regulation

**$\overline{SHDN}$ is an accurate, low-voltage logic input with 1V falling-edge threshold voltage and 1.6V rising-edge threshold voltage. ON3 and ON5 are 3-level CMOS logic inputs, a logic-low voltage is less than 0.8V, a logic-high voltage is greater than 2.4V, and the middle logic level is between 1.9V and 2.1V (see the* Electrical Characteristics *table).*

SMPS Enable Controls (ON3, ON5)

ON3 and ON5 control SMPS power-up sequencing. ON3 or ON5 rising above 2.4V enables the respective outputs. ON3 or ON5 falling below 1.6V disables the respective outputs. Driving ON_ below 0.8V clears the overvoltage, undervoltage, and thermal fault latches.

SMPS Power-Up Sequencing

Connecting ON3 or ON5 to REF forces the respective outputs off while the other output is below regulation and starts after that output regulates. The second SMPS remains on until the first SMPS turns off, the device shuts down, a fault occurs, or LDO5 goes into undervoltage lockout. Both supplies begin their power-down sequence immediately when the first supply turns off.

Output Discharge (Soft-Shutdown)

When output discharge is enabled ($\overline{OVP}$ pulled low) and the switching regulators are disabled—by transitions into standby or shutdown mode, or when an output undervoltage fault occurs—the controller discharges both outputs through internal 12Ω switches, until the output voltages decrease to 0.3V. This slowly discharges the output capacitance, providing a soft-damped shutdown response. This eliminates the slightly negative output voltages caused by quickly discharging the output through the inductor and low-side MOSFET. When an SMPS output discharges to 0.3V, its low-side driver (DL_) is forced high, clamping the respective SMPS output to GND. The reference remains active to provide an accurate threshold and to provide overvoltage protection. Both SMPS controllers contain separate soft-shutdown circuits.

When output discharge is disabled ($\overline{OVP}$ = V_{CC}), the low-side drivers (DL_) and high-side drivers (DH_) are both pulled low, forcing LX into a high-impedance state. Since the outputs are not actively discharged by the SMPS controllers, the output-voltage discharge rate is determined only by the output capacitance and load current.

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums two signals: the output-voltage error signal with respect to the reference voltage and the slope-compensation ramp (Figure 3). The MAX1533/MAX1537 use a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it. The MAX1533/MAX1537 use a relatively low loop gain, allowing the use of low-cost output capacitors. The low loop gain results in the -0.1% typical load-regulation error and helps reduce the output capacitor size and cost by shifting the unity-gain crossover frequency to a lower level.

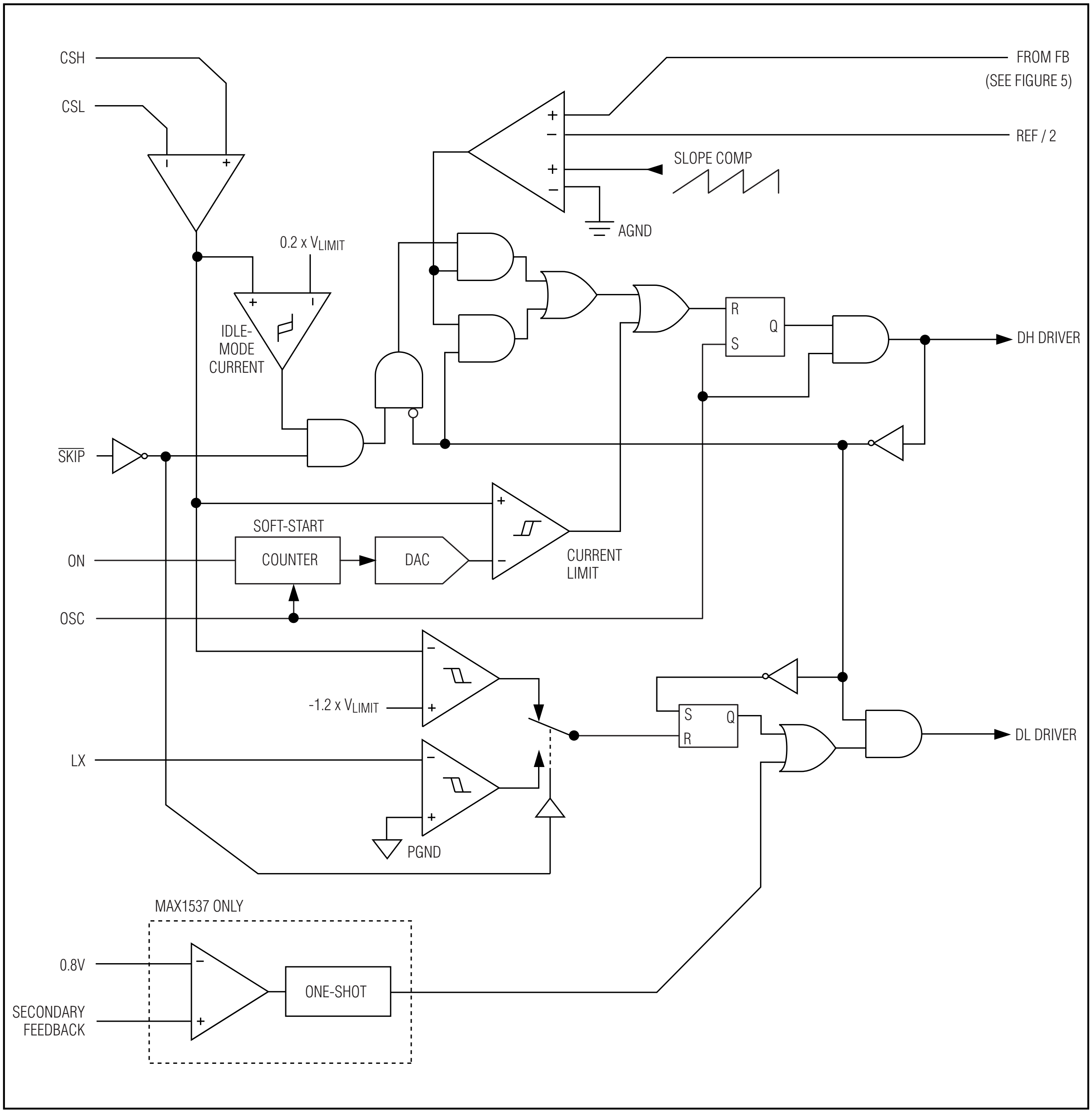


Figure 3: PWM-Controller Functional Diagram

Frequency Selection (FSEL)

The FSEL input selects the PWM-mode switching frequency. Table 4 shows the switching frequency based on FSEL connection. High-frequency (500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

Forced-PWM Mode

The low-noise forced-PWM mode disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH_ maintains a duty factor of V_{OUT} / V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V supply current remains between 15mA and 50mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for avoiding audio-frequency noise and improving load-transient response. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads.

Light-Load Operation Control ($\overline{SKIP}$)

The MAX1533/MAX1537 include a light-load operating-mode control input ($\overline{SKIP}$) used to independently enable or disable the zero-crossing comparator for both controllers. When the zero-crossing comparator is enabled, the controller forces DL_ low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. When the zero-crossing comparator is disabled, the controller is forced to maintain PWM operation under light-load conditions (forced-PWM).

Table 4. FSEL Configuration Table

FSEL	SWITCHING FREQUENCY
V_{CC}	500kHz
REF	300kHz
GND	200kHz

Idle-Mode Current-Sense Threshold

The on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle-mode current-sense threshold. Under light-load conditions, the on-time duration depends solely on the idle-mode current-sense threshold, which is approximately 20% of the full-load current-limit threshold set by ILIM_. This forces the controller to source a minimum amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until the output voltage drops below the feedback threshold. Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses. Therefore, the controller regulates the valley of the output ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 4). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFET (PGND to LX_). Once V_{PGND} - $V_{LX\_}$ drops below the 3mV zero-crossing current-sense threshold, the comparator forces DL_ low (Figure 3). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)} = \frac{V_{OUT}\,(V_{IN} - V_{OUT})}{2 \times V_{IN} \times f_{SW} \times L}$$

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

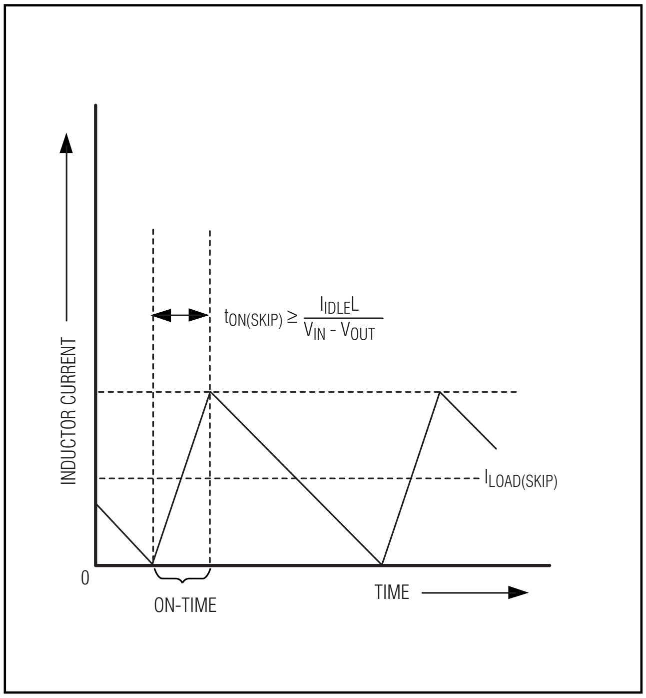


Figure 4. Pulse-Skipping/Discontinuous Crossover Point

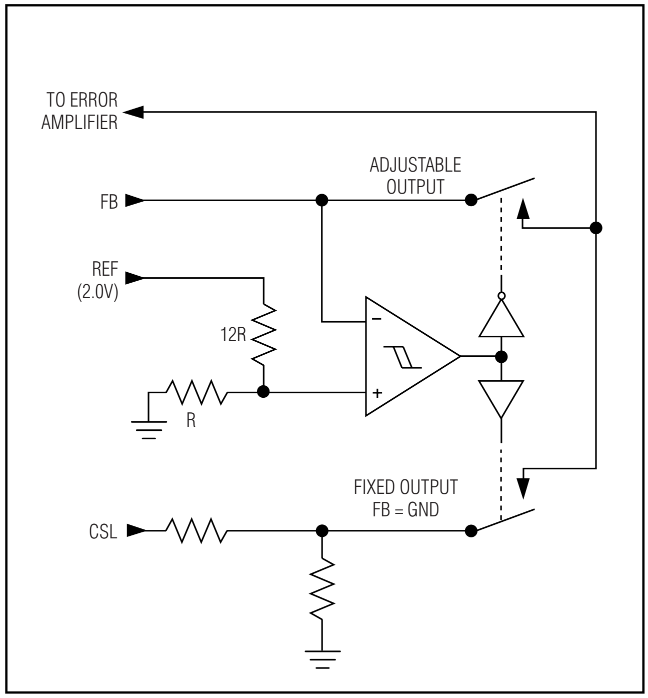


Figure 5. Dual-Mode Feedback Decoder

Output Voltage

DC output accuracy specifications in the *Electrical Characteristics* table refer to the error-comparator's threshold. When the inductor continuously conducts, the MAX1533/MAX1537 regulate the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM}\left(1 - \frac{A_{SLOPE}V_{NOM}}{V_{IN}}\right) - \left(\frac{V_{RIPPLE}}{2}\right)$$

where V_{NOM} is the nominal output voltage, A_{SLOPE} equals 1%, and V_{RIPPLE} is the output ripple voltage (V_{RIPPLE} = ESR x $\Delta I_{INDUCTOR}$ as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the MAX1533/MAX1537 regulate the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold. For PFM operation (discontinuous conduction), the output voltage is approximately defined by the following equation:

$$V_{OUT(PFM)} = V_{NOM} + \frac{1}{2}\left(\frac{f_{SW}}{f_{OSC}}\right) I_{IDLE} \times ESR$$

where V_{NOM} is the nominal output voltage, f_{OSC} is the maximum switching frequency set by the internal oscillator, f_{SW} is the actual switching frequency, and I_{IDLE} is the idle-mode inductor current when pulse skipping.

Adjustable/Fixed Output Voltages (Dual-Mode Feedback)

Connect FB3 and FB5 to GND to enable the fixed SMPS output voltages (3.3V and 5V, respectively), set by a preset, internal resistive voltage-divider connected between CSL_ and analog ground. Connect a resistive voltage-divider at FB_ between CSL_ and GND to adjust the respective output voltage between 1V and 5.5V (Figure 5). Choose R2 (resistance from FB to GND) to be about 10kΩ and solve for R1 (resistance from OUT to FB) using the equation:

$$R1 = R2\left(\frac{V_{OUT\_}}{V_{FB\_}} - 1\right)$$

where $V_{FB\_}$ = 1V nominal.

When adjusting both output voltages, set the 3.3V SMPS lower than the 5V SMPS. LDO5 connects to the 5V output (CSL5) through an internal switch only when CSL5 is above the LDO5 bootstrap threshold (4.56V). Similarly, LDO3 connects to the 3.3V output (CSL3) through an internal switch only when CSL3 is above the LDO3 bootstrap threshold (2.91V). Bootstrapping works most effectively when the fixed output voltages are used. Once LDO_ is bootstrapped from CSL_, the internal linear regulator turns off. This reduces internal power dissipation and improves efficiency at higher input voltage.

Current-Limit Protection (ILIM_)

The current-limit circuit uses differential current-sense inputs (CSH_ and CSL_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller turns off the high-side MOSFET (Figure 3). At the next rising edge of the internal oscillator, the PWM controller does not initiate a new cycle unless the current-sense signal drops below the current-limit threshold. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT} / V_{IN}).

In forced-PWM mode, the MAX1533/MAX1537 also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when ILIM_ is adjusted.

Connect ILIM_ to V_{CC} for the 75mV default threshold, or adjust the current-limit threshold with an external resistor-divider at ILIM_. Use a 2µA to 20µA divider current for accuracy and noise immunity. The current-limit threshold adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage equals precisely 1/10th the voltage seen at ILIM_. The logic threshold for switchover to the 75mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CSH_ and CSL_. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

MOSFET Gate Drivers (DH_, DL_)

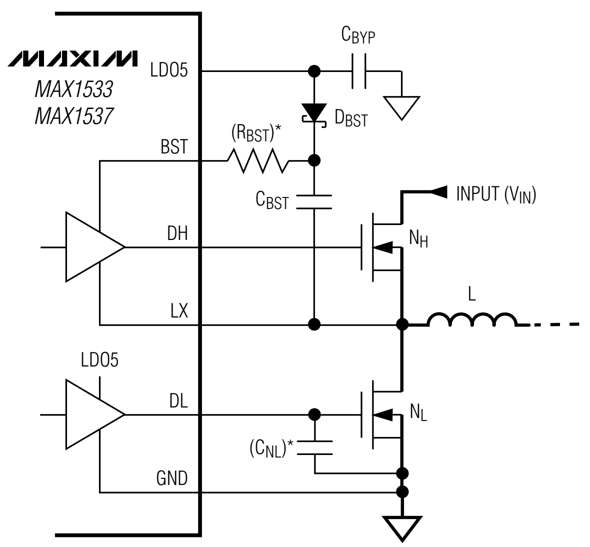
The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH_) source and sink 2A, and the low-side gate drivers (DL_) source 1.7A and sink 3.3A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by diode-capacitor charge pumps at BST_ (Figure 6) while the DL_ synchronous-rectifier drivers are powered directly by the fixed 5V linear regulator (LDO5).

Adaptive dead-time circuits monitor the DL_ and DH_ drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX1533/MAX1537 interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 to 100 mils wide if the MOSFET is 1 inch from the driver).

The internal pulldown transistor that drives DL_ low is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_ edges do not pull up the low-side MOSFETs’ gate, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFET’s gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage may cause problems in marginal designs. Alternatively, adding a resistor less than 10Ω in series with BST_ may remedy the problem by increasing the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 6).



(R_{BST})* OPTIONAL—THE RESISTOR LOWERS EMI BY DECREASING THE SWITCHING-NODE RISE TIME.
(C_{NL})* OPTIONAL—THE CAPACITOR REDUCES LX TO DL CAPACITIVE COUPLING THAT CAN CAUSE SHOOT-THROUGH CURRENTS.

Figure 6. Optional Gate-Driver Circuitry

Power-Good Output (PGOOD)

PGOOD is the open-drain output of a comparator that continuously monitors both SMPS output voltages for undervoltage conditions. PGOOD is actively held low in shutdown ($\overline{SHDN}$ or ON3 or ON5 = GND), soft-start, and soft-shutdown. Once the digital soft-start terminates, PGOOD becomes high impedance as long as both outputs are above 90% of the nominal regulation voltage set by FB_. PGOOD goes low once either SMPS output drops 10% below its nominal regulation point, an output overvoltage fault occurs, or either SMPS controller is shut down. For a logic-level PGOOD output voltage, connect an external pullup resistor between PGOOD and V_{CC}. A 100kΩ pullup resistor works well in most applications.

PGOOD is independent of the fault protection states $\overline{OVP}$ and $\overline{UVP}$.

Fault Protection

Output Overvoltage Protection (OVP)

If the output voltage of either SMPS rises above 111% of its nominal regulation voltage and the OVP protection is enabled ($\overline{OVP}$ = GND), the controller sets the fault latch, pulls PGOOD low, shuts down both SMPS controllers, and immediately pulls DH_ low and forces DL_

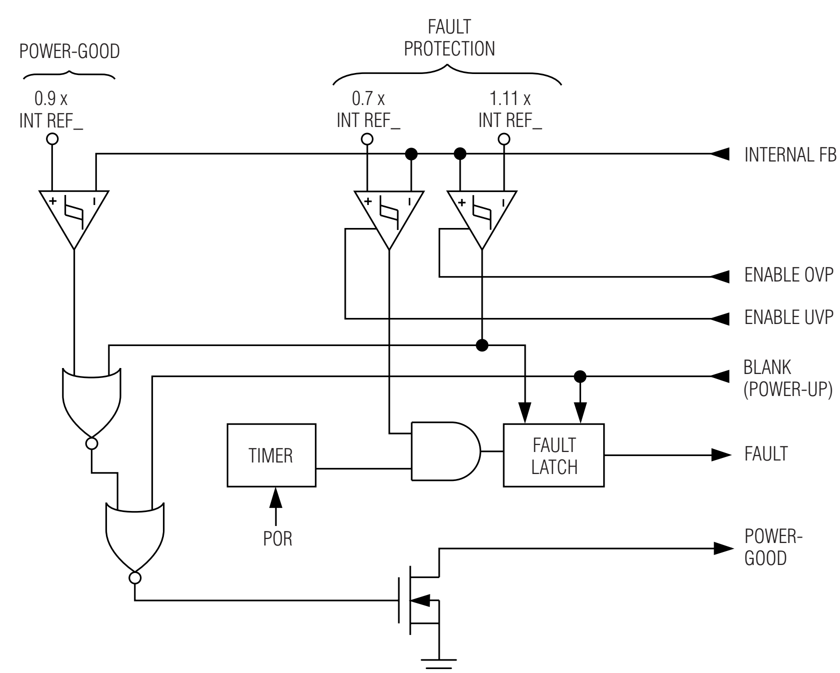


Figure 7. Power-Good and Fault Protection

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

high. This turns on the synchronous-rectifier MOSFETs with 100% duty, rapidly discharging the output capacitors and clamping both outputs to ground. However, immediately latching DL_ high typically causes slightly negative output voltages due to the energy stored in the output LC at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse blows. Cycle V_{CC} below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the SMPS controllers.

Connect $\overline{OVP}$ to V_{CC} to disable the output overvoltage protection.

Output Undervoltage Protection (UVP)

Each SMPS controller includes an output UVP protection circuit that begins to monitor the output 6144 clock cycles (1 / f_{OSC}) after that output is enabled (ON_ pulled high). If either SMPS output voltage drops below 70% of its nominal regulation voltage and the UVP protection is enabled ($\overline{UVP}$ = GND), the UVP circuit sets the fault latch, pulls PGOOD low, and shuts down both controllers using discharge mode (see the *Output Discharge (Soft-Shutdown)* section). When an SMPS output voltage drops to 0.3V, its synchronous rectifier turns on, clamping the discharged output to GND. Cycle V_{CC} below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the SMPS controllers.

Connect $\overline{UVP}$ to V_{CC} to disable the output undervoltage protection.

Table 5. Operating Modes Truth Table

MODE	CONDITION	COMMENT
Power-Up	LDO5 < UVLO threshold.	Transitions to discharge mode after V_{IN} POR and after REF becomes valid. LDO5, LDO3, REF remain active. DL_ is active if $\overline{OVP}$ is low.
Run	$\overline{SHDN}$ = high, ON3 or ON5 enabled.	Normal operation.
Output Overvoltage Protection (OVP)	Either output > 111% of nominal level, $\overline{OVP}$ = low.	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.
Output Undervoltage Protection (UVP)	Either output < 70% of nominal level, UVP is enabled 6144 clock cycles (1 / f_{OSC}) after the output is enabled and $\overline{UVP}$ = low.	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5. If $\overline{OVP}$ is not high, DL3 and DL5 go high after discharge.
Discharge	$\overline{OVP}$ is low and either SMPS output is still high in either standby mode or shutdown mode.	Discharge switch (10Ω) connects CSL_ to PGND. This is a temporary state entered when LDO5 is undervoltage or on the way to output UVLO, standby, shutdown, or thermal-shutdown states. One SMPS can be in discharge mode while the other is in run mode. If both outputs are discharged to 0.3V (on CSL_), discharge mode transitions to the appropriate state.
Standby	ON5 and ON3 < startup threshold, $\overline{SHDN}$ = high.	DL_ stays high if $\overline{OVP}$ is low. LDO3, LDO5 active.
Shutdown	$\overline{SHDN}$ = low.	All circuitry off.
Thermal Shutdown	T_J > +160°C.	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5. If $\overline{OVP}$ is not high, DL3 and DL5 go high before LDO5 turns off.
Switchover Fault	Excessive current on LDO3 or LDO5 switchover transistors.	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5. If $\overline{OVP}$ is not high, DL3 and DL5 go high before LDO5 turns off.

Thermal Fault Protection

The MAX1533/MAX1537 feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, and shuts down both SMPS controllers using discharge mode (see the *Output Discharge (Soft-Shutdown)* section). When an SMPS output voltage drops to 0.3V, its synchronous rectifier turns on, clamping the discharged output to GND. Cycle V_{CC} below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the controllers after the junction temperature cools by 15°C.

Auxiliary LDO Detailed Description (MAX1537 Only)

The MAX1537 includes an auxiliary linear regulator that delivers up to 150mA of load current. The output (LDOA) can be preset to 12V, ideal for PCMCIA power requirements, and for biasing the gates of load switches in a portable device. In adjustable mode, LDOA can be set to anywhere from 5V to 23V. The auxiliary regulator has an independent ON/OFF control, allowing it to be shut down when not needed, reducing power consumption when the system is in a low-power state.

A flyback-winding control loop regulates a secondary winding output, improving cross-regulation when the primary output is lightly loaded or when there is a low input-output differential voltage. If V_{INA} - V_{LDOA} falls below 0.8V, the low-side switch is turned on for a time equal to 33% of the switching period. This reverses the inductor (primary) current, pulling current from the output filter capacitor and causing the flyback transformer to operate in forward mode. The low impedance presented by the transformer secondary in forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing V_{INA} - V_{LDOA} back into regulation. The secondary feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this condition, secondary output accuracy is determined by the secondary rectifier drop, transformer turns ratio, and accuracy of the main output voltage.

Adjustable LDOA Voltage (Dual-Mode Feedback)

Connect ADJA to GND to enable the fixed, preset 12V auxiliary output. Connect a resistive voltage-divider at ADJA between LDOA and GND to adjust the respective output voltage between 5V and 23V (Figure 8). Choose R2 (resistance from ADJA to GND) to be approximately

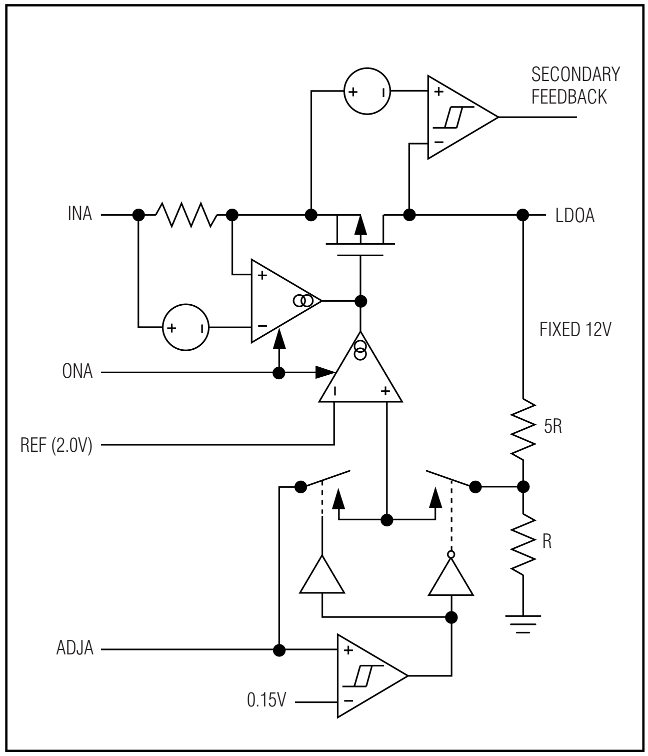


Figure 8. Linear-Regulator Functional Diagram

100kΩ and solve for R1 (resistance from LDOA to ADJA) using the following equation:

$$R1 = R2\left(\frac{V_{LDOA}}{V_{ADJA}} - 1\right)$$

where V_{ADJA} = 2V nominal.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery-selector switches. If there is a choice at all, lower input voltages result in better efficiency.

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

- **Maximum Load Current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output-capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}\, f_{OSC}\, I_{LOAD(MAX)}\, LIR}$$

For example: $I_{LOAD(MAX)}$ = 5A, V_{IN} = 12V, V_{OUT} = 5V, f_{OSC} = 300kHz, 30% ripple current or LIR = 0.3.

$$L = \frac{5V \times (12V - 5V)}{12V \times 300kHz \times 5A \times 0.3} = 6.50\mu H$$

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}\; f_{OSC}\; L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Transformer Design (For the MAX1537 Auxiliary Output)

A coupled inductor or transformer can be substituted for the inductor in the 5V SMPS to create an auxiliary output (Figure 1). The MAX1537 is particularly well suited for such applications because the secondary feedback threshold automatically triggers DL5 even if the 5V output is lightly loaded.

The power requirements of the auxiliary supply must be considered in the design of the main output. The transformer must be designed to deliver the required current in both the primary and the secondary outputs with the proper turns ratio and inductance. The power ratings of the synchronous-rectifier MOSFETs and the current limit in the MAX1537 must also be adjusted accordingly. Extremes of low input-output differentials, widely different output loading levels, and high turns ratios can further complicate the design due to parasitic transformer parameters such as interwinding capacitance, secondary resistance, and leakage inductance. Power from the main and secondary outputs is combined to get an equivalent current referred to the main output. Use this total current to determine the current limit (see the *Setting the Current Limit* section):

$$I_{TOTAL} = P_{TOTAL} / V_{OUT5}$$

where I_{TOTAL} is the equivalent output current referred to the main output, and P_{TOTAL} is the sum of the output power from both the main output and the secondary output:

$$N = \frac{V_{SEC} + V_{FWD}}{V_{OUT5} + V_{RECT} + V_{SENSE}}$$

where $L_{PRIMARY}$ is the primary inductance, N is the transformer turns ratio, V_{SEC} is the minimum required rectified secondary voltage, V_{FWD} is the forward drop across the secondary rectifier, $V_{OUT5(MIN)}$ is the minimum value of the main output voltage, and V_{RECT} is the on-state voltage drop across the synchronous-rectifier MOSFET. The transformer secondary return is often connected to the main output voltage instead of ground to reduce the necessary turns ratio. In this case, subtract V_{OUT5} from the secondary voltage (V_{SEC} - V_{OUT5}) in the transformer turns-ratio equation above. The secondary diode in coupled-inductor applications must withstand flyback voltages greater than 60V. Common silicon rectifiers, such as the 1N4001, are also prohibited because they are too slow. Fast silicon rectifiers such as the MURS120 are the only choice. The flyback voltage across the rectifier is related to the V_{IN} - V_{OUT} difference, according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT5}) \times N$$

where N is the transformer turns ratio (secondary windings/primary windings), and V_{SEC} is the maximum secondary DC output voltage. If the secondary winding is returned to V_{OUT5} instead of ground, subtract V_{OUT5} from $V_{FLYBACK}$ in the equation above. The diode's reverse-breakdown voltage rating must also accommodate any ringing due to leakage inductance. The diode's current rating should be at least twice the DC load current on the secondary output.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output voltage sag is the sum of the voltage sag while the inductor is ramping up, and the voltage sag before the next pulse can occur.

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2C_{OUT}\left(V_{IN} \times D_{MAX} - V_{OUT}\right)} + \frac{\Delta I_{LOAD(MAX)}\left(T - \Delta T\right)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor (see the *Electrical Characteristics* table), T is the switching period (1 / f_{OSC}), and ΔT equals V_{OUT} / V_{IN} x T when in PWM mode, or L x 0.2 x I_{MAX} / (V_{IN} - V_{OUT}) when in skip mode. The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT}\ V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The peak inductor current occurs at $I_{LOAD(MAX)}$ plus half the ripple current; therefore:

$$I_{LIMIT} > I_{LOAD(MAX)} + \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

where I_{LIMIT} equals the minimum current-limit threshold voltage divided by the current-sense resistance (R_{SENSE}). For the default setting, the minimum current-limit threshold is 70mV.

Connect ILIM_ to V_{CC} for the default current-limit threshold. In adjustable mode, the current-limit threshold is precisely 1/10th the voltage seen at ILIM_. For an adjustable threshold, connect a resistive divider from REF to analog ground (GND) with ILIM_ connected to the center tap. The external 500mV to 2V adjustment range corresponds to a 50mV to 200mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10µA to prevent significant inaccuracy in the current-limit tolerance.

The current-sense method (Figure 9) and magnitude determine the achievable current-limit accuracy and power loss. Typically, higher current-sense limits provide tighter accuracy, but also dissipate more power. Most applications employ a current-limit threshold (V_{LIMIT}) of 50mV to 100mV, so the sense resistor can be determined by:

$$R_{SENSE} = V_{LIMIT} / I_{LIM}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 9a. This configuration constantly monitors the inductor current, allowing accurate current-limit protection.

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

Alternatively, high-power applications that do not require highly accurate current-limit protection may reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 9b) with an equivalent time constant:

$$\frac{L}{R_L} = C_{EQ} \times R_{EQ}$$

where R_L is the inductor's series DC resistance. In this configuration, the current-sense resistance equals the inductor's DC resistance ($R_{SENSE} = R_L$). Use the worst-case inductance and R_L values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors (see the *Output-Capacitor Stability Considerations* section),

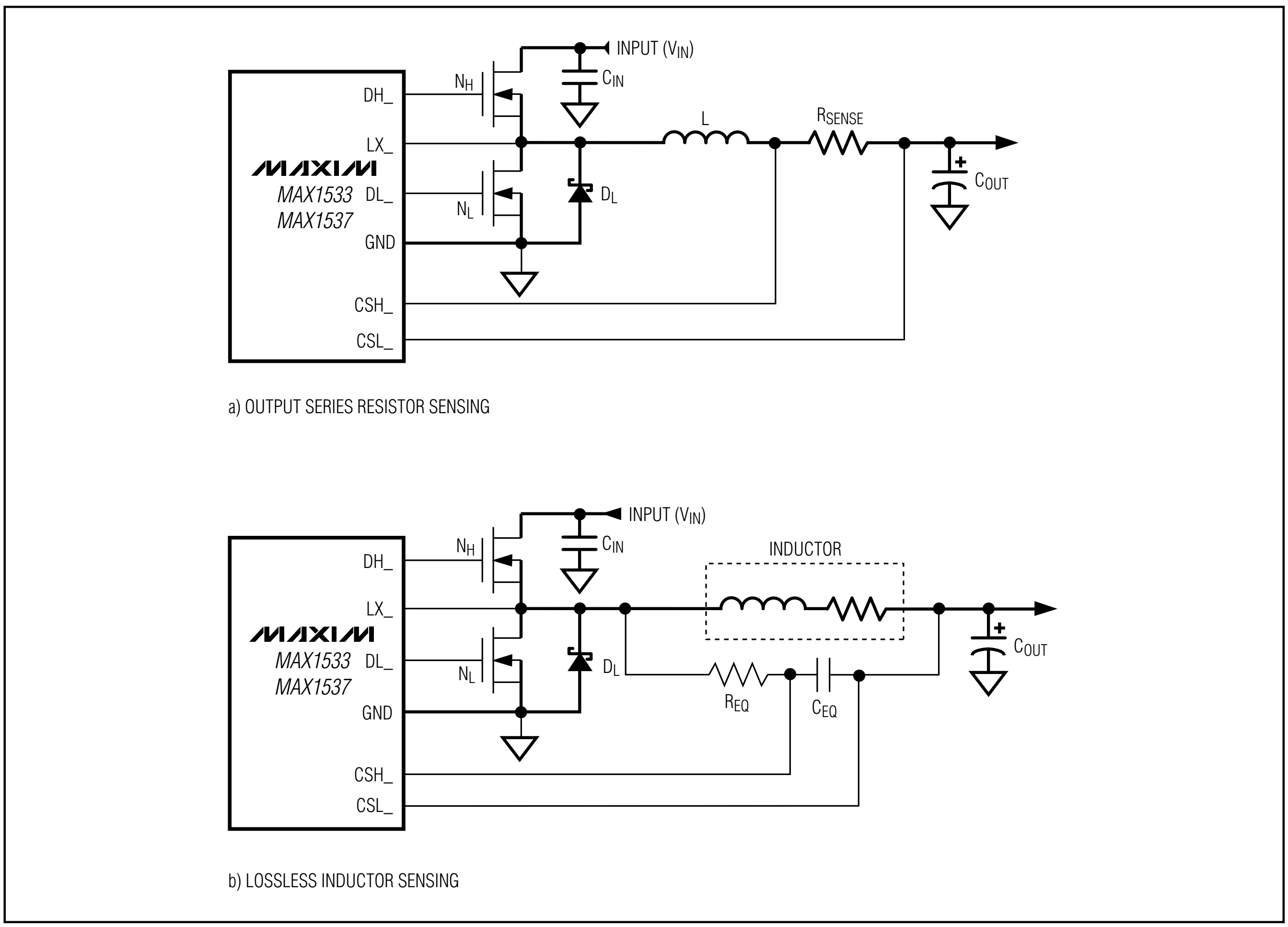


Figure 9. Current-Sense Configurations

the filter capacitor's ESR dominates the output voltage ripple. So the output capacitor's size depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = R_{ESR} I_{LOAD(MAX)} LIR$$

In idle mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-sense threshold ($V_{IDLE} = 0.2V_{LIMIT}$). In idle mode, the no-load output ripple can be determined as follows:

$$V_{RIPPLE(P-P)} = \frac{V_{IDLE} R_{ESR}}{R_{SENSE}}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics). When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that may affect the overall stability (see the *Output-Capacitor Stability Considerations*).

Output-Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{OSC}}{\pi}$$

$$\text{where } f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support $25mV_{P-P}$ ripple is 25mV / 1.5A = 16.7mΩ. One 220µF/4V Sanyo polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

For low-input-voltage applications where the duty cycle exceeds 50% ($V_{OUT} / V_{IN} \ge 50\%$), the output ripple voltage should not be greater than twice the internal slope-compensation voltage:

$$V_{RIPPLE} \le 0.02 \times V_{OUT}$$

where V_{RIPPLE} equals $\Delta I_{INDUCTOR} \times R_{ESR}$. The worst-case ESR limit occurs when $V_{IN} = 2 \times V_{OUT}$, so the above equation can be simplified to provide the following boundary condition:

$$R_{ESR} \le 0.04 \times L \times f_{OSC}$$

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: short/long pulses or cycle skipping resulting in a lower switching frequency. Instability occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering too early or skipping a cycle. Cycle skipping is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC-current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. For an out-of-phase regulator, the total RMS current in the input capacitor is a function of the load currents, the input currents, the duty cycles, and the amount of overlap as defined in Figure 10.

The 40/60 optimal interleaved architecture of the MAX1533/MAX1537 allows the input voltage to go as low as 8.3V before the duty cycles begin to overlap.

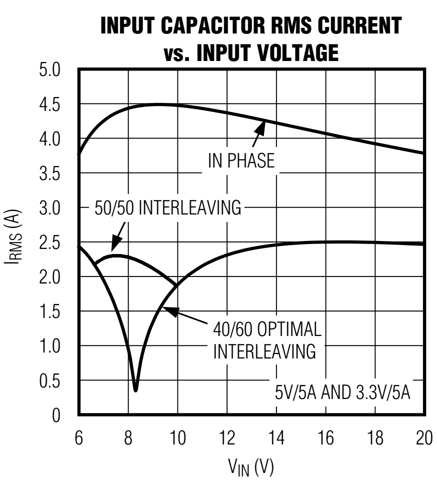
This offers improved efficiency over a regular 180° out-of-phase architecture where the duty cycles begin to overlap below 10V. Figure 10 shows the input-capacitor RMS current vs. input voltage for an application that requires 5V/5A and 3.3V/5A. This shows the improvement of the 40/60 optimal interleaving over 50/50 interleaving and in-phase operation.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. Choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.



INPUT RMS CURRENT FOR INTERLEAVED OPERATION

$$I_{RMS} = \sqrt{(I_{OUT5} - I_{IN})^2 (D_{LX5} - D_{OL}) + (I_{OUT3} - I_{IN})^2 (D_{LX3} - D_{OL}) + (I_{OUT5} + I_{OUT3} - I_{IN})^2 D_{OL} + I_{IN}^2 (1 - D_{LX5} - D_{LX3} + D_{OL})}$$

$$D_{LX5} = \frac{V_{OUT5}}{V_{IN}} \quad D_{LX3} = \frac{V_{OUT3}}{V_{IN}} \quad D_{OL} = \text{DUTY-CYCLE OVERLAP FRACTION}$$

INPUT RMS CURRENT FOR SINGLE-PHASE OPERATION

$$I_{RMS} = I_{LOAD} \left(\frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}} \right)$$

Figure 10. Input RMS Current

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., SO-8, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX1533/MAX1537 DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power-MOSFET Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD\ (N_H\ \text{Resistive}) = \left(\frac{V_{OUT}}{V_{IN}} \right) (I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ \text{Switching}) = \frac{(V_{IN(MAX)})^2 C_{RSS}\ f_{SW}\ I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N_H, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC-adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\ (N_L\ \text{Resistive}) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy-overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT} - \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

where I_{LIMIT} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward-voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3rd the load current. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{Q_{GATE}}{200mV}$$

where Q_{GATE} is the total gate charge specified in the high-side MOSFET's data sheet. For example, assume the FDS6612A n-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single FDS6612A has a maximum gate charge of 13nC (V_{GS} = 5V). Using the above equation, the required boost capacitance is:

$$C_{BST} = \frac{13nC}{200mV} = 0.065\mu F$$

Selecting the closest standard value. This example requires a 0.1µF ceramic capacitor.

Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by the maximum duty-cycle specification (see the *Electrical Characteristics* table). However, keep in mind that the transient performance gets worse as the step-down regulators approach the dropout voltage, so bulk output capacitance must be added (see the voltage sag and soar equations in the *Design Procedure* section). The absolute point of dropout occurs when the inductor current ramps down during the off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). This results in a minimum operating voltage defined by the following equation:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + h\left(\frac{1}{D_{MAX}} - 1\right)(V_{OUT} + V_{DIS})$$

where V_{CHG} and V_{DIS} are the parasitic voltage drops in the charge and discharge paths, respectively. A reasonable minimum value for h is 1.5, while the absolute minimum input voltage is calculated with h = 1.

Maximum Input Voltage

The MAX1533/MAX1537 controllers include a minimum on-time specification, which determines the maximum input operating voltage that maintains the selected switching frequency (see the *Electrical Characteristics* table). Operation above this maximum input voltage results in pulse-skipping operation, regardless of the operating mode selected by $\overline{SKIP}$. At the beginning of each cycle, if the output voltage is still above the feedback-threshold voltage, the controller does not trigger an on-time pulse, effectively skipping a cycle. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{OSC} \quad t_{ON(MIN)}}\right)$$

where f_{OSC} is the switching frequency selected by FSEL.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 11). If possible, mount all of the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSH_ and CSL_ directly across the current-sense resistor ($R_{SENSE\_}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, FB_, CSH_, CSL_).

Layout Procedure

1) Place the power components first, with ground terminals adjacent ($N_{L\_}$ source, C_{IN}, $C_{OUT\_}$, and $D_{L\_}$ anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite $N_{L\_}$ and $N_{H\_}$ to keep LX_, GND, DH_, and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 to 100 mils wide if the MOSFET is 1 inch from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
3) Group the gate-drive components (BST_ diode and capacitor, LDO5 bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figures 1 and 11. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
5) Connect the output power planes directly to the output-filter-capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

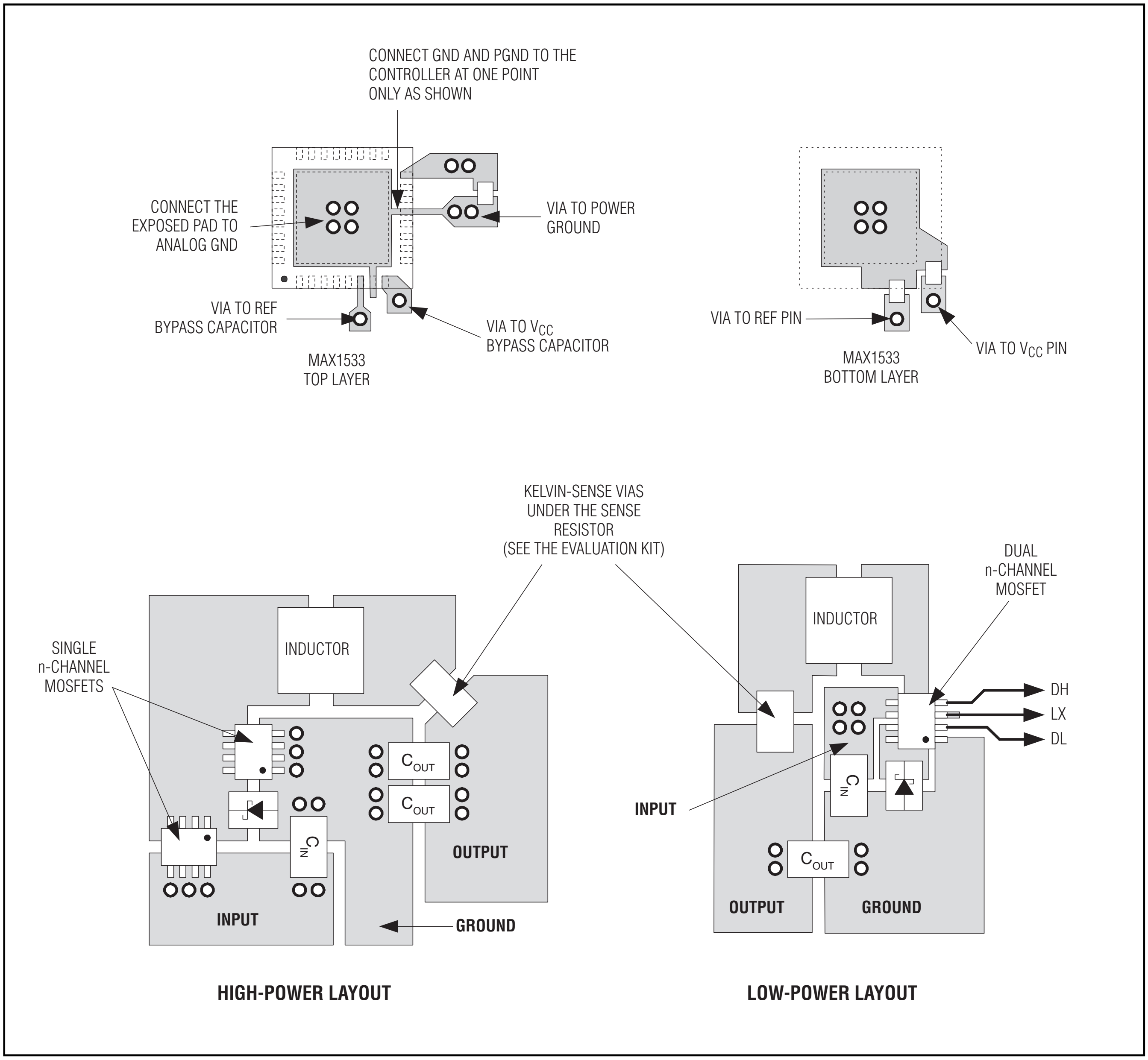
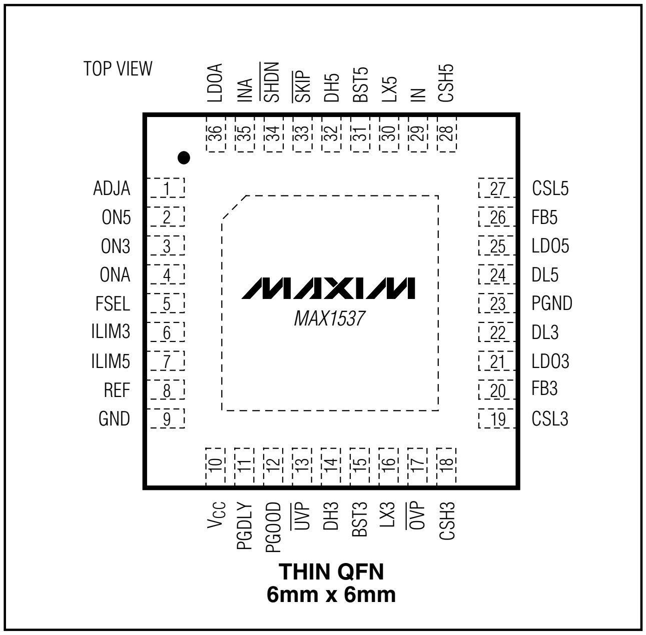


Figure 11. PC Board Layout

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

Pin Configurations (continued)



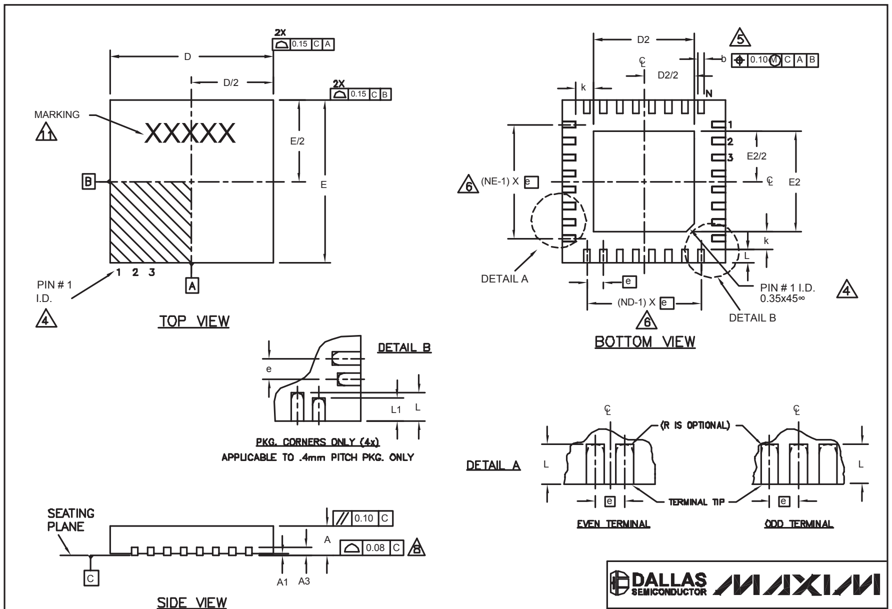
Chip Information

TRANSISTOR COUNT: 6890

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	F	1/2

-DRAWING NOT TO SCALE-

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

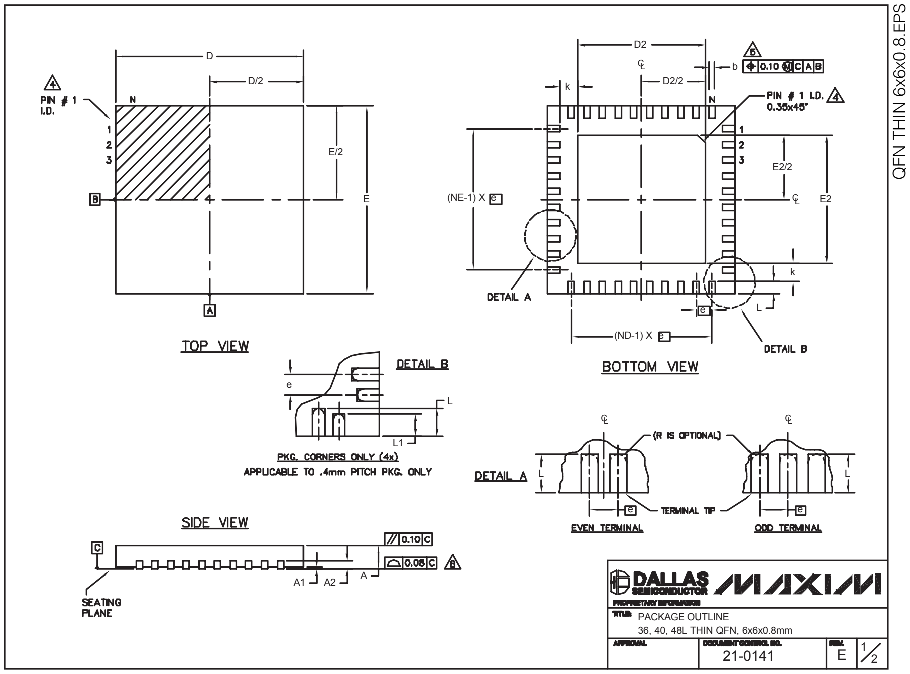
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	F	2/2

High-Efficiency, 5x Output, Main Power-Supply Controllers for Notebook Computers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

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5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	E	2/2

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